

INSTRUCTION MANUAL

**MODELS 605, 606
PROGRAMMABLE
WAVEFORM GENERATORS**

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IF YOUR INSTRUMENT DOES NOT OPERATE

PLEASE

1. Check operating procedure in manual for proper setup.
2. Check fuse and power supply voltages.
3. Call your Exact representative or factory. Instruments returned to the factory will be accepted only if they are sent freight prepaid, unless Exact or factory representative has authorized otherwise.

CLAIM FOR DAMAGED SHIPMENT

The instrument should be inspected as soon as received. If damage has occurred, a claim should be made with the carrier. The claim agent should receive a complete report of damage and a copy sent to Exact. After receiving this report, Exact will advise you of the disposition of the instrument and arrange for its repair or replacement.

WARRANTY

Exact warrants its instruments to be free from defects in material and workmanship under normal use for a period of twelve months from the original date of shipment. Exact's obligation is limited to repair or replacement.

All repairs and replacements made under this warranty are f.o.b. Exact's factory or designated service depot unless otherwise authorized by Exact. This warranty is made on condition that prompt notice of defect is given to Exact, in writing, within the warranty period and that Exact shall have the sole right to determine whether in fact a defect exists.

This warranty does not apply to any instrument which has been repaired or altered by other than Exact's own service representative so as, in Exact's judgment, to adversely affect it, nor which has been subject to misuse, negligence or accident or which has been operated contrary to sound practice or operating instructions.

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INTRODUCTION

SECTION 2

2.1.0 INTRODUCTION

The Exact models 605 and 606 programmable waveform generators were designed to fulfill the need for accurate waveform generation, controlled by an external system or controller such as a digital computer. These generators can be completely controlled for amplitude, Frequency, Function, Triggering, Offset, and Start phase by an external source. The external programming source can be a contact closure such as a rotary switch or a relay. It can be a signal from TTL or DTL logic systems or it can be any other electrical signal within the operating range of the program inputs. The external programming source can be electrically isolated from the generator's circuit common. The Model 605 has provisions for locally controlling all functions, frequencies and amplitudes as well as external or Remote mode.

The program inputs are on the rear panel in a single 50-pin receptacle. All other generator inputs and outputs "sync, VCF, etc" are also available on the rear of this 3 1/2" high regular rack width package. The part number for the mating plug to the 50-pin receptacle is Amphenol 57-30500.

This manual is an attempt to provide complete information on the specifications, operational procedures, circuit description, calibration, parts list, schematics, etc. of the Exact models 605 and 606. The information in this manual remains the property of Exact Electronics, Inc. and shall not be used or copied without the express permission of same. Patent Pending.

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SECTION 3

SPECIFICATIONS

AND

VERIFICATION OF SPECIFICATIONS PROCEDURE

3.1.0 SPECIFICATIONS

DYNAMIC FREQUENCY RANGE

The instrument will operate over a frequency range from .001Hz to 1 MHz with front panel controls. It will also operate up to 1.6 MHz with 60% overrange of the 1248 BCD programming when programmed externally.

Decade frequency ranges are:

1	-	10	milliHz	100	-	1000	Hz
10	-	100	milliHz	1	-	10	KHz
100	-	1000	milliHz	10	-	100	KHz
1	-	10	milliHz	100	-	1000	KHz
10	-	100	milliHz				

Front panel vernier frequency control covers the range of 1 least significant bit (605 only).

FREQUENCY ACCURACY

- ± 1% of setting + 1 digit between 0.01 Hz and 100 KHz
- ± 2% of setting + 1 digit between 0.001 Hz and 0.01 Hz.
- ± 2% of setting + 1 digit between 100 KHz and 1 MHz.

FREQUENCY STABILITY

0.04% of setting for 10 minutes, 0.2% for 24 hours.

VCF (Voltage Controlled Frequency)

External frequency control with D. C. or A. C. (usable to 1 MHz). Positive input increases and negative input decreases frequency from programmed value. Nominal input 5V for 1600:1 into 5K input impedance.

WAVEFORMS

Basic Function selection produces Sine, Triangle, Square, Ramp, Pulse and Sine-Squared waveforms.

Run, Gate, Trigger - Any of the basic waveforms can be produced continuously by selecting the Run Mode. Selecting Gate or Trigger Mode will cause the generator to lockout at zero degrees starting phase for the Sine, Triangle, and Ramp waveforms, and at the peak values for pulse or square. Sine-Squared locks out at - 90°. All waveforms can be inverted 180°.

Application of an external or manual Gate/Trigger command when in the Triggered Mode will produce 1 complete cycle of the selected waveform. In the Gate Mode the generator will continue to produce the output waveforms until the command is removed.

Gate/Trigger signal requirements are TTL - DTL compatible. Requires approximately 1.2 volts into a 10K ohm input impedance.

D. C. OFFSET

Programmed waveform is decreased to half its peak to peak amplitude and offset so that one peak is maintained at zero volts.

EXTERNAL D. C. OFFSET

Rear panel input that accepts D. C. or A. C. signals to be summed with the selected waveform. Normal 1:1 inverting relationship on the 1 - 10V P-P range is attenuated by selecting lower voltage ranges.

TRIANGLE MONITOR OUTPUT

Fixed Triangle or Ramp waveform of 10V P-P-open circuit with 600 Ω output impedance.

SYNC OUT

Square Waveform of approximately 4V P-P with an output impedance of 100 Ω . Square transitions are coincident with the Triangle, Ramp, and Sine peaks or the Square and Pulse transitions.

OUTPUT VOLTAGE

1 millivolt to 10 volts P-P into 50 Ω load in four ranges with 3 digit setability.

1	-	10	millivolts peak to peak into 50 Ω
10	-	100	millivolts "
100	-	1000	millivolts "
1	-	10	volts "

With D. C. Offset

0.5	-	5	mv peak into 50 Ω
5	-	50	mv "
50	-	500	mv "
0.5	-	5	v "

External programming with the 1248 BCD code provides overranging of 60% to produce a maximum of 16V peak to peak. (Slewing rate limits prevent overranging frequency and voltage at the same time, 100 KHz and above).

PHASE LOCK INPUT

A signal of 5V P-P applied to this input will synchronize the instrument when the frequencies are within approximately 1%.

PROGRAMMING

The programming inputs are compatible with TTL, DTL contact closure and etc. Current sink is less than 1 ma. Programming time is less than 0.5 milliseconds.

There are 38 programming inputs plus program common which is isolated from instrument common.

INPUTS:

Frequency Decade	4 inputs	BCD
Frequency Control	12 inputs	BCD 3 digits
Voltage Control	12 inputs	BCD 3 digits
Voltage Range	2 inputs	Binary
Polarity (waveform)	1 input	Binary
D.C. Offset (fixed)	1 input	Binary
Mode Run, Gate, Trigger	2 inputs	Binary
Function (waveform)	4 inputs	Binary

SIZE

3 1/2" high x 17" wide (19" in rackmount) x 13 1/2" deep.
Rackmounting adapters supplied.

Power input requirements are 117 or 200 volts A.C. \pm 10% 50 - 400 Hz, other voltages available. 100, 200, 234 specify.

All instrument specifications apply after a 30 minute warmup time at 25°C \pm 5°C ambient temperature. To maintain specifications unit must be operated between 10% and 100% of maximum amplitude and frequency ranges.

3.2.0 VERIFICATION OF SPECIFICATIONS

The following is a list of test equipment required to validate the specifications of the Models 605 and 606 Programmable Waveform Generators. Test equipment of the accuracy equal to or better than the following list is acceptable for specification validation.

Oscilloscope, D.C. to 50 MHz (Tektronix Model 544)
 Plug-In Differential Comparator 10 millivolts per centimeter sensitivity (Tektronix Type W)
 Counter/Timer . μ sec time base, DANA 8010B
 DVM .01% Accuracy DANA 4300
 Harmonic Distortion Analyzer less than .1% residual distortion (Hewlett Packard Model 333)
 Spectrum Analyzer 10KHz to 100MHz (Nelson Ross plug-in for Type 544)

To proceed with verification of specifications, program the generator as follows:
 800Hz on the 100 to 999Hz range, free running Normal phase sine wave of 8.00V P-P with no offset and the delta frequency control to CAL, Model 605 only. The Model 605 can be locally programmed for the same conditions.

3.2.1 FREQUENCY STABILITY

Connect the output of the generator to the frequency counter and observe that the frequency remains within .04% for ten minutes or $\pm .5\mu$ sec time interval.

3.2.2 FREQUENCY ACCURACY

Frequency should be 800Hz within 1% + 1 digit or 809Hz to 791Hz.
 Reprogram for 400Hz, frequency should be within 1% + 1 digit or 405Hz to 395Hz
 Reprogram for 200Hz, frequency should be within 1% + 1 digit or 203Hz to 197Hz
 Reprogram for 100Hz, frequency should be within 1% + 1 digit or 102Hz to 98Hz
 Reprogram for 880Hz, frequency should be within 1% + 1 digit or 889.8Hz to 870.2Hz
 Reprogram for 840Hz, frequency should be within 1% + 1 digit or 849.4Hz to 830.6Hz
 Reprogram for 820Hz, frequency should be within 1% + 1 digit or 829.2Hz to 810.8Hz
 Reprogram for 810Hz, frequency should be within 1% + 1 digit or 819.1Hz to 800.9Hz
 Reprogram for 808Hz, frequency should be within 1% + 1 digit or 817.1Hz to 798.9Hz
 Reprogram for 804Hz, frequency should be within 1% + 1 digit or 813Hz to 795Hz
 Reprogram for 802Hz, frequency should be within 1% + 1 digit or 811Hz to 793Hz
 Reprogram for 801Hz, frequency should be within 1% + 1 digit or 810Hz to 792Hz

Reprogram frequency for 800Hz, set Decade Multiplier to the bottom range, that is the 1 to 9.99mHz range. Verify the frequency as 8mHz $\pm 2\%$ + 1 digit or from 8.17mHz to 7.83mHz. Program up one range and verify the frequency as 80mHz $\pm 1\%$ + 1 digit or 80.9Hz to 79.1Hz. Program up one range and verify that the frequency is 800mHz $\pm 1\%$ + 1 digit or 809mHz to 791mHz. Program up one range and verify that the frequency is 8Hz $\pm 1\%$ + 1 digit or 8.09Hz to 7.91Hz. Program up one range and verify that the frequency is 80Hz $\pm 1\%$ + 1 digit or 80.9Hz to 79.1Hz. Program up one range and verify that the frequency is 800Hz $\pm 1\%$ + 1 digit or 809Hz to 791Hz. Program up one range and verify that the frequency is 8KHz $\pm 1\%$ + 1 digit or 8.09KHz to 7.91KHz. Program up one range and verify that the frequency is 80KHz $\pm 1\%$ + 1 digit or 80.9KHz to 79.1KHz. Program up one range and verify that the frequency is 800KHz $\pm 2\%$ + 1 digit or 817KHz to 783KHz.

3.2.3 AMPLITUDE ACCURACY (Note: Output must be properly terminated in 50.0Ω)

Reprogram generator for frequency of 800Hz and using comparison oscilloscope, check the amplitude accuracy at 8.00V P-P into 50.0Ω to be within $\pm 1\%$ + 1 digit or 8.09V to 7.91V. Reprogram output voltage for 4.00V and check that amplitude is within $1\% \pm 1$ digit or 4.05V to 3.95V. Reprogram output voltage for 2.00V P-P and check to see that amplitude is within $1\% \pm 1$ digit or 2.03V to 1.97V. Reprogram for 1.00V P-P output and check to see that amplitude is within $1\% + 1$ digit or 1.02V to .98V. Reprogram for output voltage of 8.80V P-P and check to see that amplitude is within $1\% + 1$ digit or 8.898V to 8.702V. Reprogram for 8.4V and check to see that output is within $1\% + 1$ digit or 8.494V to 8.306V. Reprogram for 8.20V P-P and check to see that amplitude is within $1\% + 1$ digit or 8.292V to 8.108V. Reprogram for 8.10V P-P and see that output amplitude is within $1\% + 1$ digit or 8.191V to 8.109V. Reprogram output voltage for 8.01V P-P and check to see that amplitude is within $1\% + 1$ digit or 8.10V to 7.92V. Reprogram output amplitude for 8.02V P-P and see that amplitude is within $1\% + 1$ digit or 811V to 793V. Reprogram for 8.04V P-P and see that amplitude is within $1\% + 1$ digit or 811V to 793V. Reprogram for 8.08V P-P and check to see that amplitude is within $1\% + 1$ digit or 8.171V to 7.989V. Return program to 8.00V P-P and program generator for frequency of 999KHz and check to see that amplitude is within 5% or 8.40V to 7.60V.

3.2.4 SINE FREQUENCY RESPONSE

Program generator for 9.99KHz sine wave of 8.00V P-P, measure amplitude accurately and record. Program generator for 99.9KHz sine wave and verify that amplitude is within .1db (1.14% or 90mv) of reading obtained at 9.99KHz. Program generator for frequency of 999KHz and measure amplitude to verify that it is within .5db (5.6% or 448mv) of the value obtained at 9.99KHz.

3.2.5 AMPLITUDE STABILITY

Program generator for frequency of 800Hz and an output amplitude of 8.00V P-P, measure amplitude and record and then again at ten minutes and check to see that amplitude is within .05% (4mv) of reading obtained previously.

3.2.6 SINE WAVE DISTORTION

Program generator for a sine wave output of 9.99V P-P at a frequency of 9.99KHz. Connect distortion analyzer to the main output jack and measure sine distortion of less than .5%. Reprogram generator for frequency of 99.9KHz and measure sine distortion of less than .5%. Reprogram generator for frequency of 999KHz. Connect Spectrum Analyzer to Main Output jack and measure harmonic content. Observe no harmonics less than 30db down.

3.2.7 SQUARE WAVEFORM

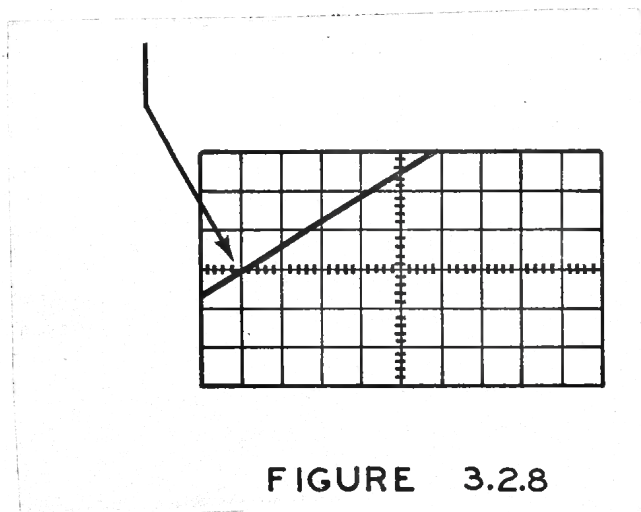
Program generator for 999KHz square wave positive or negative of 9.99V P-P. Connect main output through 50Ω coaxial cable terminated into 50Ω to the oscilloscope. Observe

3.2.7 (Continued)

rise time and fall time of square is less than 100ns between 10% to 90% points. Observe overshoot and ringing is less than 5% of P-P amplitude (.50V ringing or overshoot).

3.2.8 TRIANGLE LINEARITY (Refer figure 3.2.8)

Connect the Main Output to a differential plug-in with 50 Ω coaxial cable terminated in 50 Ω . Adjust oscilloscope to obtain one-half cycle triangle across horizontal grid on oscilloscope CRT. Set differential plug-in sensitivity to 20mv per centimeter. Adjust comparison voltage until the slope of the triangle waveform intersects the mid-scale horizontal grid line at the second major mark as shown below.



Record reference voltage using DVM accurate to 1mv. Adjust comparison voltage until slope of triangle intersects next major horizontal grid mark. Record accurately the new reference voltage. Repeat to obtain as many points as desired. Calculate linearity and observe linearity is 99% or better to 100KHz, 95% or better to 1.09MHz. Beware of oscilloscope inadequacies above 100KHz.

SECTION 4

OPERATING INSTRUCTIONS

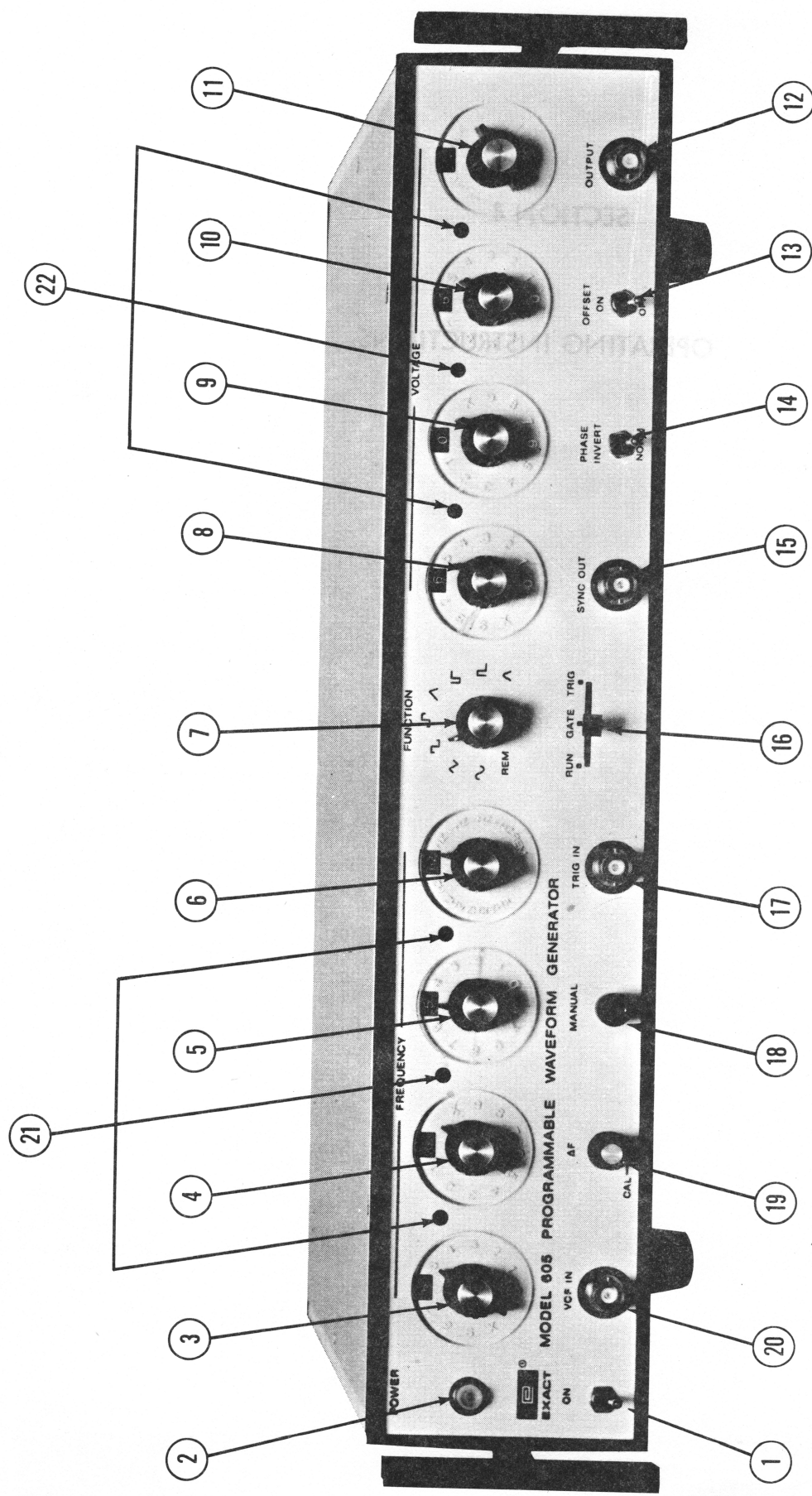


FIGURE 4.1.1
FRONT PANEL MODEL 605

4.1.0 FRONT PANEL FAMILIARITY (Figure 4.1.1)

1. Power On/Off switch - turns on input power to instrument.
2. Pilot Lamp - indicates input power On.
3. Frequency Multiplier - hundreds digit.
4. Frequency Multiplier - tens digit.
5. Frequency Multiplier - units digit.
6. Frequency Decade range selector - allows operation over nine decade frequency range.
7. Function selector - selects waveform to appear at the output connectors.
8. Voltage Multiplier - hundreds digit.
9. Voltage Multiplier - tens digit.
10. Voltage Multiplier - units digit.
11. Voltage Decade range selector - allows operation over four decade voltage range.
12. Output connector - allows 50Ω output impedance for generated waveform.
13. Offset control - decreases program waveform to $1/2$ programmed amplitude and offsets same to a level equal to its peak amplitude so that one peak is maintained at 0 volts.
14. Phase control - provides for 180 degree phase inversion of output waveform.
15. Sync output connector - provides square waveform for synchronizing other equipment to the generator.
16. Trigger mode control - selects free running, gated, or triggered operation.
17. Trigger input connector - accepts gating or trigger signals.
18. Manual Trigger control - allows manual gating or triggering of generator.
19. Delta Frequency control - allows vernier adjustment of frequency.
20. VCF input connector - accepts analog voltage for control of generated frequency.
21. Automatic decimal point indicators - operated by the Frequency Decade range control.
22. Automatic decimal point indicators - operated by the Voltage Decade range control.

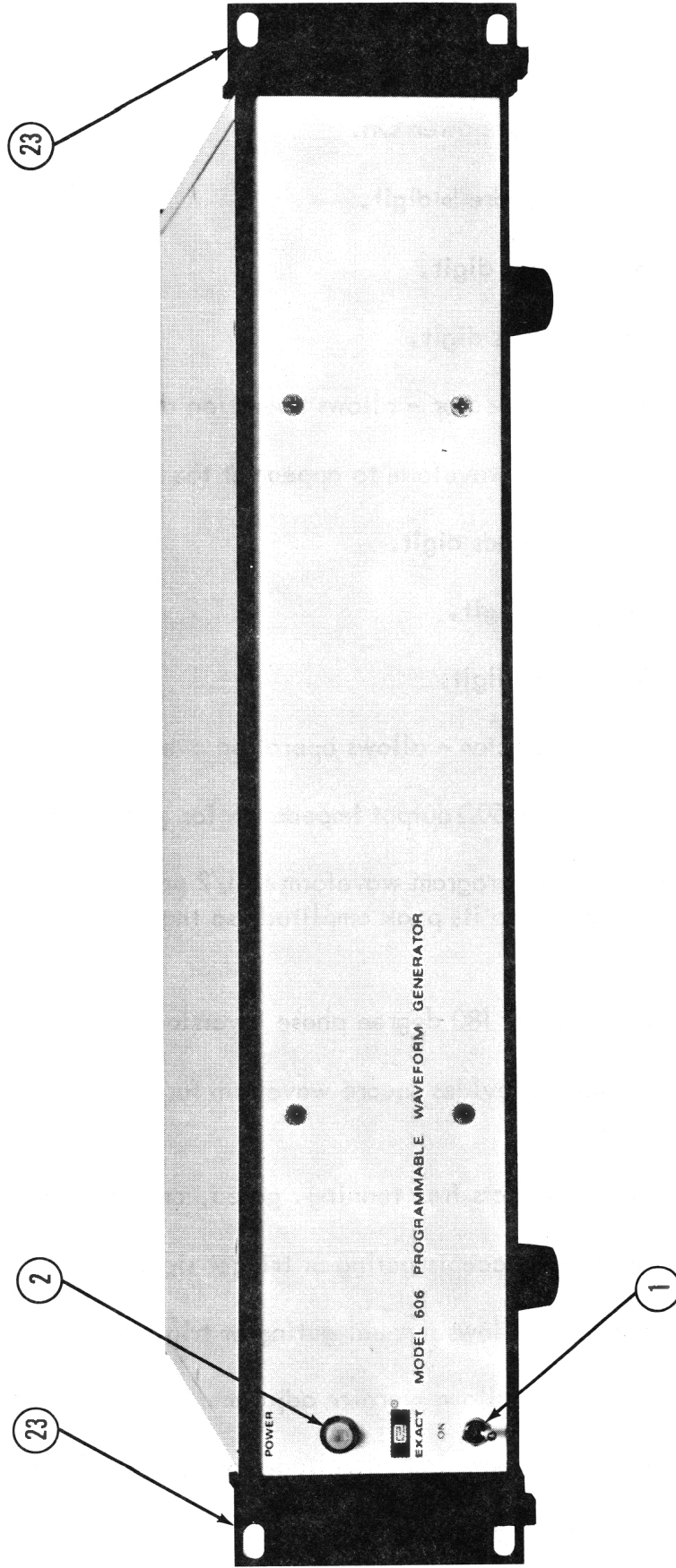


FIGURE 4.1.2
FRONT PANEL MODEL 606

4.1.2 FRONT PANEL FAMILIARITY (Figure 4.1.2)

1. Power On/Off switch - turns on input power to instrument.
2. Pilot Lamp - indicates input power On.
3. Rack mounting - standard equipment.



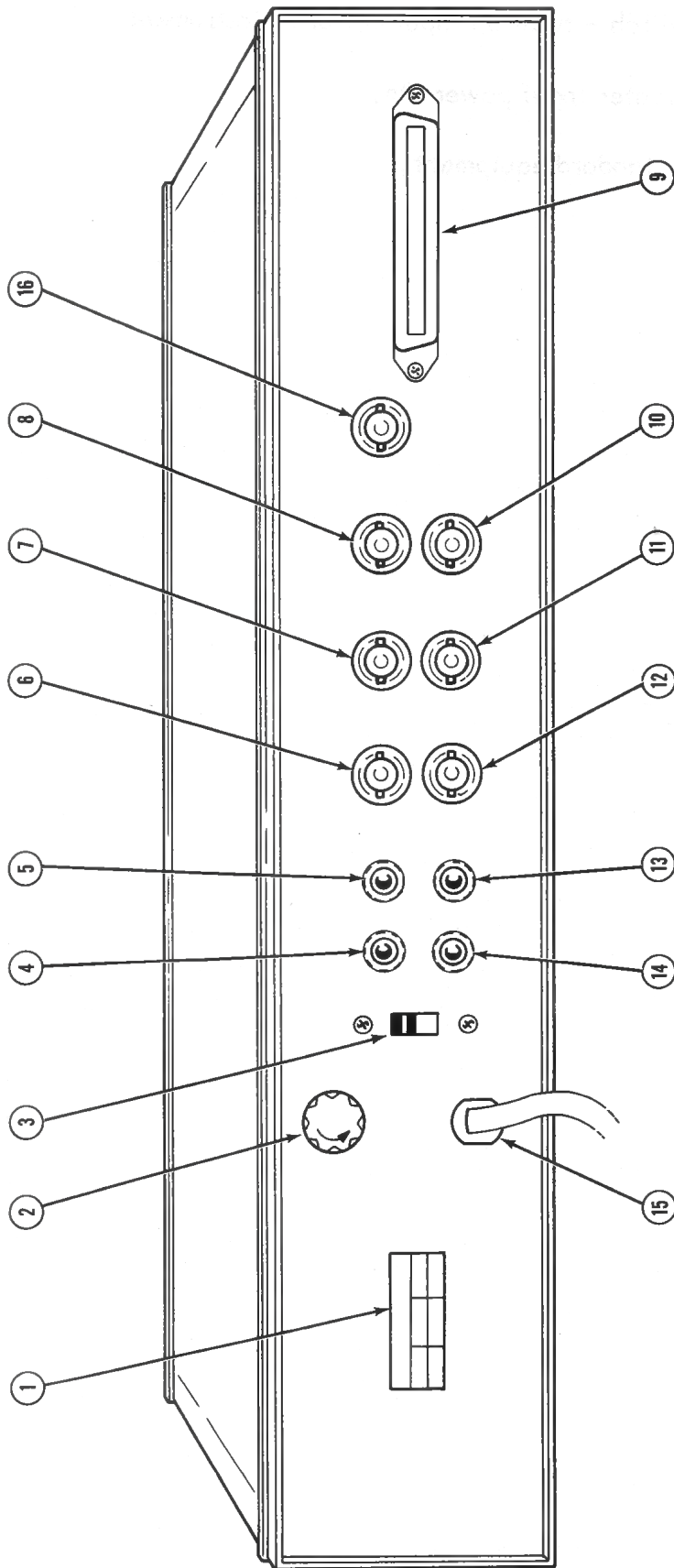


FIGURE 4.2.1
 REAR PANEL MODEL 605-606

4.2.0 REAR PANEL FAMILIARITY (Refer figure 4.2.1)

1. Fuse data chart - shows requirements for operation at 115 or 220 volts.
2. Fuse holder - allows easy replacement in the event of fuse failure.
3. Line voltage selector - allows instrument operation from 110 or 220 volts AC.
4. Circuit Common connection - allows floating Circuit Common operation of instrument.
5. Programming Common connection - allows floating operation of the Programming circuitry.
6. Output connector - main output of generator.
7. DC Offset input connector - accepts external analog signal for programming D.C. offset.
8. Sync output connector - provides signal for synchronizing other equipment such as oscilloscopes, etc.
9. Programming input connector - accepts program inputs for remote control of the generator.
10. Trigger input connector - accepts input signals for gating or triggering of generator.
11. VCF input connector - accepts wideband AC or DC input for analog programming of generator frequency.
12. Triangle Monitor connector - provides constant monitor of triangle or ramp waveform generated in the instrument.
13. Chassis ground connection - provides for grounding of program common.
14. Chassis ground connection - provides for grounding of circuit common.
15. Line cord - accepts input power of the instrument.
16. Phase lock - accepts input synchronizing signal.

4.3.0 PROGRAMMING REQUIREMENTS

The circuitry at the programming inputs consists of a single transistor with a diode switching bridge on the base input.

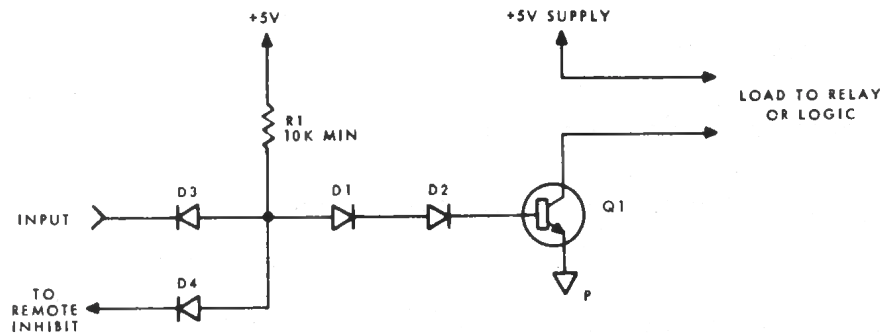


FIGURE 4.3.1

The transistor Q1 is used as a saturated switch for operation of reed relays and also as direct input for the TTL logic in the instrument. Resistor R1 provides the necessary base current for transistor Q1 through diodes D1 and D2. As either the input or the remote/inhibit bus is held low (programming ground or up to $-50V$), the current supplied from R1 is shunted out through the input diode D3 and D4. Without base current for Q1, collector current does not flow, and the relay or logic system is not energized. As the input is held positive (above 1.4V nominal), current from R1 begins to flow through D1 and D2 turning on Q1's collector current and activating its relay or logic circuitry. Some of the possible combinations of circuitry that can be used to operate the inputs are contact closure, DTL, TTL, direct voltage application and etc. One requirement of programming sources is that it must be capable of holding the low level state while sinking the 1 milliamp (nominal) of current being supplied by R1 (refer figure as previous). Maximum value of resistance to hold the input to a low stage should be 1.6K Ω .

An almost limitless list of combinations exists with the inputs' capability of handling $\pm 50V$ DC and the switch point being at +1.2V nominal, in reference to the programming common. Some combinations are shown below:

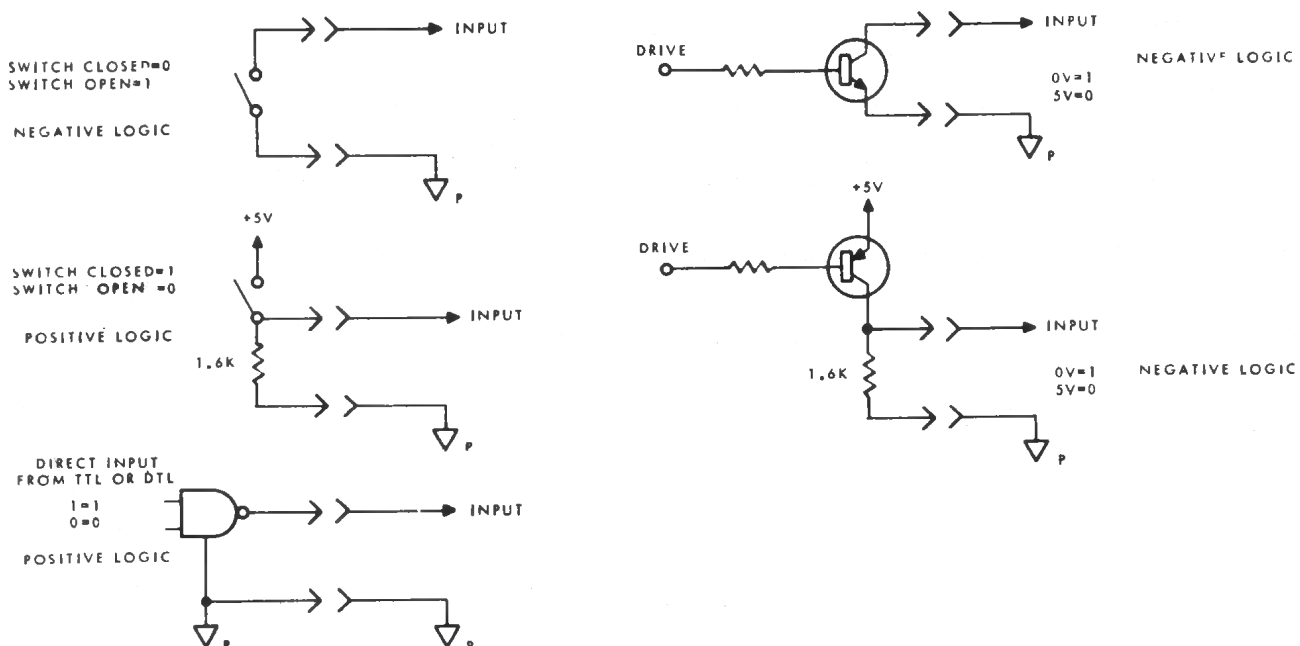


FIGURE 4.3.2

4.4.0 PROGRAMMING TABLES

The Models 605 and 606 have thirty-eight active inputs for programming output waveforms. With a logical "0" being defined as +.4V or less and logical "1" being defined as +2.4V or more, a truth table can be shown for generator control in response to logical "0's" and "1's". In the Model 605, the inputs and controls are grouped into three groups so that any one of the three groups can be controlled remotely or locally. Any group can be operated in either control mode without affecting the others. The three groups are as follows: frequency, function (includes trigger mode, invert and offset), and voltage. Of the three groups, "frequency" has a total of sixteen external inputs. "Function" has eight inputs and "voltage" has fourteen inputs.

4.4.1 Of the sixteen inputs listed under "Frequency", four are used to control the decade range and twelve are used to control the multiplier.

The decoding for the decade range is as follows:

Decimal Eq.	Pin Number for Programming Input Connector				Frequency Range
	43	42	41	40	
0	0	0	0	0	1 - 10 mHz
1	0	0	0	1	10 - 100 mHz
2	0	0	1	0	100 - 1000 mHz
3	0	0	1	1	1 - 10 Hz
4	0	1	0	0	10 - 100 Hz
5	0	1	0	1	100 - 1000 Hz
6	0	1	1	0	1 - 10 KHz
7	0	1	1	1	10 - 100 KHz
8	1	0	0	0	100 - 1000 KHz
Binary Weight	8	4	2	1	

Binary weight and decimal equivalents apply to standard 1-2-4-8 BCD or straight binary only.

4.4.1 (Continued)

The decoding for the multiplier is as follows:

Decimal Eq.	Pin Number Program Input Connector													
	28	29	30	31		32	33	34	35		36	37	38	39
0	0	0	0	0	0	0	0	0	0	0	0	0	0	
100	0	0	0	1	10	0	0	0	1	1	0	0	0	
200	0	0	1	0	20	0	0	1	0	2	0	0	1	
300	0	0	1	1	30	0	0	1	1	3	0	0	1	
400	0	1	0	0	40	0	1	0	0	4	0	1	0	
500	0	1	0	1	50	0	1	0	1	5	0	1	0	
600	0	1	1	0	60	0	1	1	0	6	0	1	1	
700	0	1	1	1	70	0	1	1	1	7	0	1	1	
800	1	0	0	0	80	1	0	0	0	8	1	0	0	
900	1	0	0	1	90	1	0	0	1	9	1	0	0	
X00	1	0	1	0	X0	1	0	1	0	X	1	0	1	
Binary Weight	8	4	2	1		8	4	2	1		8	4	2	

Binary weight and decimal equivalent apply to standard 1248 BCD codes only.

- 4.4.2 The eight inputs used to program functions can be broken down into several groups, some of which have only a single function as compared to others which are used in a sequence. The groups are trigger mode control (two inputs), polarity inversion (one input), fixed offset (one input), and waveform (four inputs).

4.4.2 (Continued)

The decoding table for the trigger mode control is as follows:

Decimal Eq.	Pin Number of Program Input Connector		
	27	26	
0	0	0	Inhibit External Triggering (Avail. as Option)
1	0	1	Trigger
2	1	0	Gate
3	1	1	Run
Binary Weight	2	1	

The decoding for the polarity inversion input is as follows:

Decimal Eq.	Pin Number of Program Input Connector		
	5		
0	0	0	Normal Output Polarity
1	1	1	Inverted Output
Binary Weight	1		

The decoding for the fixed offset input is as follows:

Decimal Eq.	Pin Number of Program Input Connector		
	3		
0	0	0	Fixed Offset
1	1	1	Normal Waveform
Binary Weight	1		

4.4.2 (Continued)

Decoding for the waveform inputs is as follows:

Decimal Eq.	Pin Number of Program Input Connector				
	4	44	1	2	
8	1	0	0	0	Sine
9	1	0	0	1	Triangle
10	1	0	1	0	Normal Square
11	1	0	1	1	INV Square
14	1	1	1	0	INV Pulse
15	1	1	1	1	Normal Pulse
0	0	0	0	0	90 Degree Sine
5	0	1	0	1	Ramp
Binary Weight	8	4	2	1	

4.4.2 (Continued)

The decoding table for the "voltage" multiplier is as follows:

Decimal Eq.	Pin Number Program Input Connector													
	6	7	8	9		10	11	12	13		14	15	16	17
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
100	0	0	0	1	10	0	0	0	1	1	0	0	0	1
200	0	0	1	0	20	0	0	1	0	2	0	0	1	0
300	0	0	1	1	30	0	0	1	1	3	0	0	1	1
400	0	1	0	0	40	0	1	0	0	4	0	1	0	0
500	0	1	0	1	50	0	1	0	1	5	0	1	0	1
600	0	1	1	0	60	0	1	1	0	6	0	1	1	0
700	0	1	1	1	70	0	1	1	1	7	0	1	1	1
800	1	0	0	0	80	1	0	0	0	8	1	0	0	0
900	1	0	0	1	90	1	0	0	1	9	1	0	0	1
X00	1	0	1	0	X0	1	0	1	0	X	1	0	1	0
Binary Weight	8	4	2	1		8	4	2	1		8	4	2	1

Binary weight and decimal equivalent apply to standard 1248 BCD codes only.

The decoding for the "Voltage Decade" is as follows

Decimal Eq.	Pin Number of Prog. Input		
	19	18	
0	0	0	1-10mv
1	0	1	10-100mv
2	1	0	100-1000mv
3	1	1	1-10V
Binary Weight	2	1	

- 4.4.3 Pin #50 of the program input connector is the common return for all programming input connections. Pin #25 of the program input connector is a supply of +5V suitable for supplying logical "1's" to inputs held low with resistors.
- 4.4.4 Representative program might be as follows: generate a free running 925Hz inverted triangle (no offset) at 678mv P-P.

Frequency Group

	Pin Number Program Input Connector															
	28	29	30	31	32	33	34	35	36	37	38	39	43	42	41	40
Binary Weight	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1
Necessary Input	1	0	0	1	0	0	1	0	0	1	0	1	0	1	1	0
Actual Output	9			2				5			X 100 to 1000Hz Range = 925Hz					

Function Group

	Pin Number of Program Input Connector							
	27	26	5	3	4	44	1	2
Binary Weight	2	1	1	1	8	4	2	1
Necessary Input	1	1	1	1	1	0	0	1
	Run	Inv.	Nc	Offset	Triangle			

Voltage Group

	Pin Number of Input Connector													
	18	19	6	7	8	9	10	11	12	13	14	15	16	17
Binary Weight	2	1	8	4	2	1	8	4	2	1	8	4	2	1
Necessary Input	1	0	0	1	1	0	0	1	1	1	1	0	0	0
Actual Output	100-1000mv Range		X	6	7					8 = 678mv				

In the Model 605, it is necessary to set the frequency decade control, the function selector, and voltage to the Remote position for complete remote programming as is the foregoing.

4.4.5 LOCAL OPERATION, MODEL 605

In order to generate the free-running 925Hz inverted triangle with no offset at 678mv P-P (as in the previous example), it is necessary to preset the control knobs as follows: With the power switch on, preset the frequency multiplier to the digits 925 as indicated in the program and rotate the decade selector until the automatic decimal point indicates that you have selected 925Hz. Select Triangle on the function selector and also set the phase switch to the Inverted position. Preset the trigger mode selector to Run for free-running waveform. Next it is necessary to select the digits 6, 7 and 8 on the voltage multiplier and then rotate the voltage decade selector until the automatic decimal indicator indicates that you have selected 678mv. Monitoring the output connector at this point and time should verify that indeed you have generated the required waveform as set forth in the program.

SECTION 5

CIRCUIT DESCRIPTION

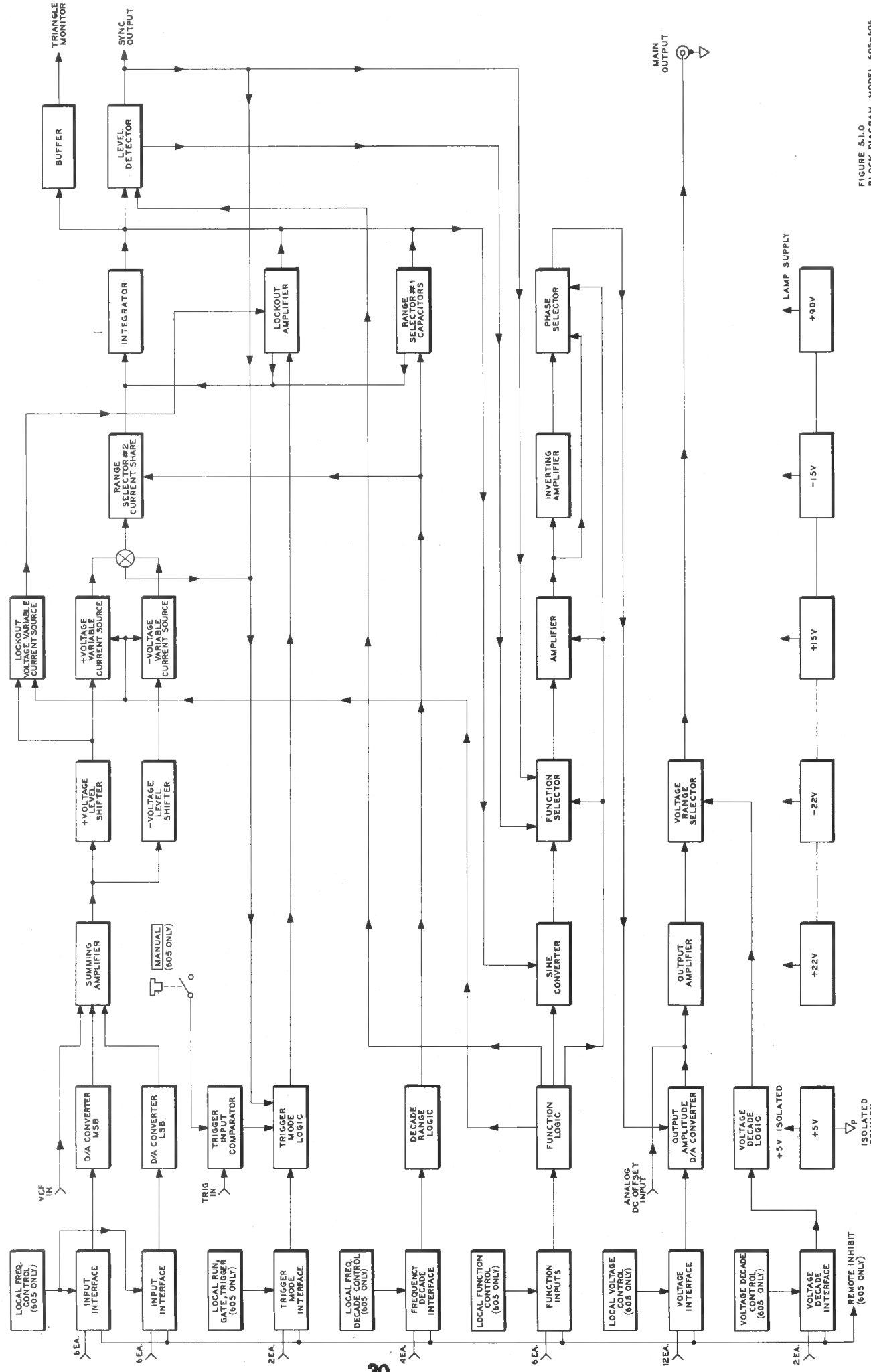


FIGURE 5.1.0
BLOCK DIAGRAM MODEL 605-606
11-18-70

5.1.0 BLOCK DIAGRAM (Refer Figure 5.1.0)

The basic generator loop utilized in this generator is an operational integrator and a bi-stable level detector. The bi-stable level detector switches integrator input currents at predetermined points on the integrator output. The loop generates a constant amplitude triangle whose frequency is proportional to the integrator input current and integrator feedback capacitance. Decade values of frequency are selected by decade selection of feedback capacitance and for the lower ranges decade selection of current sharing network on the input of the integrator. Variable frequency adjustment is accomplished by having voltage variable current sources feeding into the current switch at the input of the integrator. These voltage variable current sources are in actuality operational current sources driven by two operational voltage level shifters which are driven by the single summing amplifier. The summing amplifier is used to provide an external analog programming of frequency (VCF) or it is used to sum the outputs of the two amplifiers used to provide the digital analog conversion. The digital to analog conversion is done in two sections so that each section can be operated at a higher current level and therefore neither one has to operate at extremely low current levels. D to A conversion is done through a series of relay closures providing different resistance value for each weighting of an input. The relay activation is provided by the interface circuitry which is a saturated transistor switch operated by an external input signal.

The basic generator loop (the integrator and level detector) by nature provides a triangular waveform and a square waveform that can be processed and used as output signals to provide two waveforms. The triangular wave can be processed through the sine converter and provide a sinusoidal waveform. All three of these waveforms then are supplied to the function selector which is controlled by the function logic circuitry. The function logic circuitry decodes the input of the six function inputs such that each waveform can be provided for a given input condition at the function inputs. The output of the function selector is applied to the amplifier which provides a constant output amplitude and at the same time provides for the offset half amplitude function. The output of this amplifier is fed to the phase selector and also the inverting amplifier. The output of the inverting amplifier is fed to the phase selector. Phase selector is controlled by the function logic so that either output phase from the main generator loop can be provided to the output amplifier. The output of the phase selector is fed to the output amplitude D to A converter. The output D to A converter is a series of relays and different values of input resistors for the output amplifier. These relays are activated by the output amplitude interface circuitry which is the input circuitry for the external programming. The output amplifier accepts the signals from the output D to A converter and converts them to output voltage for the voltage range selector. The output amplifier provides the power necessary for driving a 50Ω output impedance. Voltage range selector is a series of 20db attenuator pads. These attenuator pads are controlled by the voltage decade logic circuitry. The voltage decade logic circuitry decodes the inputs from the voltage decade interface for selection of the correct voltage range. The interface circuitry provides conditioning for the external programming input signals.

There are six power supplies in the Models 605 and 606; one of the power supplies being a +5V supply that is completely isolated from the other power supplies. The +5V supplies

5.1.0 (Continued)

all the logic circuitry and interface circuitry associated with the external programming. The +22 and -22 supplies are used to provide voltage for the current sources and the output amplifier. The +15 and -15 are re-regulated from the +22V and -22V. They are used to provide operating voltages for other circuitry in the generator loop. +90V supply is used to power the pilot lamps and the automatic decimal point lamps in the instruments.

5.2.0 POWER SUPPLY (Refer Figure 8.2.1)

The power line voltage is fed to the instrument through Plug P100 to the protective fuse F100. The line switch S100 supplies line voltage to the operating voltage selector S101. S101 applies the voltage to the transformer in either a series or parallel arrangement depending on the line voltage available. The transformer T100 is used to step down the voltages to lower values for application to the rectifier filter combinations in the instrument. Diodes D100 and D105 in combination with capacitors C101 provide an unregulated voltage of approximately 9.8V to supply the integrated circuit regulator Q100. Q100 is a complete power supply inside an integrated circuit package. It contains its own reference, voltage supply, and error amplifier. Q105 is an external series pass transistor used to enhance the current carrying capabilities of Q100. R105 is a current sensing resistor used to supply current limiting voltages to the integrated circuit Q100. Resistive divider R100, R101 and R102 is used to provide the necessary feedback voltage to the error amplifier inside Q100. R101 provides for a small adjustment in the value of the output voltage. Diode D105 prevents any external application of negative voltage to any of the circuitry on the +5V programming power supply lines.

With all of the TTL logic and logic interface circuitry, etc. connected to the +5V power supply, an overvoltage would be somewhat catastrophic; therefore, a completely passive "Crowbar" circuit has been installed. Any overvoltage on the +5V power supply line in excess of 10% will cause Q115, a silicon control rectifier, to conduct and remain conducting until the overvoltage has been corrected. The power switch must be turned off and then on again to restore operation. SCR Q115 receives its gate current drive from transistor Q110. Transistor Q110 is operated as a saturated switch. It gets its base drive from tunnel diode D110. Tunnel diode D110 is biased near its peak point current by resistor R111 and adjustment R112. Resistor R110 is used to increase the amount of voltage drop across the base emitter junction so that it is adequate to turn on Q110. The programming supply +5V and its common are isolated from instrument common and also from line ground or chassis ground. If needed, these connections can be made through rear panel jacks J102 and J103. Rear panel jacks J101 and J100 also provide connection of circuit common which is also isolated to chassis ground.

Full wave diode bridge D120 along with filter capacitors C120 and C140 provides approximately $\pm 30V$ for the regulators that regulate to +22 and -22V. Integrated circuit Q120 is a power supply unit that contains its own reference error amplifier and etc. Transistor Q125 is used to enhance the current carrying capability of the integrated circuit. Resistor R125 provides the current sensing so that the integrated circuit can be used to provide current limiting. Feedback voltage for the error amplifier in the

5.2.0 (Continued)

integrated circuit is developed across voltage divider R126, R127 and R128. Adjustment R127 is used to provide a small amount of voltage adjustment for the +22V supply. Diode D125 provides protection against accidental applications of negative voltages to the +22V power supply line. The +22V supply is used as a reference for the discrete component regulator that generates the -22V. Divider R156, R157 and R158 applies this reference to the differential amplifier made up of transistors Q150 and Q155. The base of transistor Q150 is held at 0V by resistor R150. The output of the differential pair (which appears at the collector of Q150) is applied to the base of transistor Q140 through resistor R151. Capacitor C141 and resistor R142 are phase compensating networks for the regulator. The output of transistor Q140 is applied to resistor R145 which in turn is connected to the base of the series pass transistor Q145. The emitter of Q145 supplies the necessary output current through current sensing resistor R145 to the power supply output. Transistor Q160 is used to provide a feedback signal to the differential amplifier Q155 through diode D160. This turns power supply voltage off in the event of a current limit signal which is developed across R145. Feedback necessary for power supply operation is through resistor R158 which maintains the reference to Q155 at 0V when both the power supplies are equal and opposite. Adjustment R157 provides for small amount of adjustment in the output voltage of the -22V supply. Diode D160 prevents damage in the event of application of positive voltage to the -22V power supply line. To provide a very stable 15V supply, the +22V from regulator Q120 is applied to integrated circuit Q130 and is re-regulated. Q130 is a complete power supply in one integrated circuit; that is, it has its own reference, error amplifier, etc. Transistor Q135 is used to enhance the current carrying capabilities of the integrated circuit. Resistor R135 is a current sensing resistor used to provide current limit operation of the integrated circuit. Feedback necessary for closed loop operation is through resistive divider made up of R136, R137 and R138. Adjustment R137 is used to provide a small amount of variation in the value of the supply voltage obtained at +15V supply output. Diode D135 is used to prevent damage in the event of application of negative voltage to the +15V power supply line. Operational amplifier Q165 is used as an inverting amplifier with a gain of 1 to provide a negative 15V power supply that tracks very accurately the positive 15V power supply. Diode D165 is used to shift the level of the operational amplifier to a higher voltage for operation of the Darlington circuit made up of transistors Q170, Q175. The output of the series pass transistor Q175 is applied to the -15V line through current sensing resistor R175. Transistor Q180 is used to provide a feedback signal when current limit is reached. This feedback signal is applied to the input of the operational amplifier and reduces its output in the event of a current limit. Feedback necessary for closed loop operation is through R167, adjustment R166, and R165 to the +15V supply. Adjustment R166 is used to provide the small range of adjustment in the output voltage of the -15V supply. Diode D175 is used to prevent damage in the event of an application of the positive voltage to the -15V line. Diode D10, D11, D12 and D13, in conjunction with capacitor C10, are used to provide a supply of positive 90V DC. This supply is used to operate the instrument power on lamp and the automatic decimal point indicating lamps on the front panel of the Model 605.

5.3.0 GENERATOR LOOP CIRCUITRY (Refer Figure 8.2.2)

The integrator portion of the generator loop circuitry can best be described as an operational amplifier utilizing capacitors as feedback network, therefore can be termed an operational integrator. This operational amplifier has two signal paths, one covering the range DC to 100KHz and the other covering the range 100KHz and above. Transistor Q340 being a matched dual field effect transistor comprises the input circuitry for the low frequency path in the amplifier. This circuit is a differential amplifier whose outputs are applied to another differential amplifier made up of Q355, Q360. The voltage developed across voltage dividers R347 thru R351 and including R344 is used to offset the differential voltage between the two gate connections of the dual transistor Q340. The output of this second differential pair (the collector of transistor Q340) is applied to the base of one of the transistors used in the differential mixer (transistors Q365 and Q370). The input for the high frequency channel is transistor Q350. The signal from Q350 is applied to the other input of the differential mixer (the base of Q370). One polarity of output from the differential mixer (the collector of Q365) is applied to the base of Q375 through phase compensating network C365 and R366. Transistor Q375 inverts this signal and it becomes the same polarity as the opposite output of the differential mixer. These two signals are then connected together through bias diodes D375 and D370 and including resistor R370 to the output emitter followers transistors Q380 and Q385. The emitter followers Q380 and Q385 provide a very low value of output impedance for the operational amplifier. Diodes D371 and D376 provide short circuit protection for the output devices in this amplifier.

The feedback capacitors necessary to form the operational integrator from the operational amplifier is a matched set of capacitors C435A through C435E. For the higher ranges, a small variable capacitor with a parallel fixed capacitor (C436 and C437) is used. The input current for the integrator is applied to the current sharing networks. The current sharing networks are only used for the three lower ranges of the instrument. For all other ranges, a "short to summing junction relay" is turned on and the current is applied directly to the input of the operational integrator. Diodes D319A and B are a matched pair. Diodes D320A and B are also a matched pair. These four diodes are used to short the output of the integrator to the input and to lock out the Integrator-Level detector loop and stop operation of both. Diodes D315 and D316 are used to sink the current from the lock-out current source when it is not desired to lock out the integrator level detector loop. Differential pair Q315 and Q320 are used to control these diodes when the signal from the integrated circuit Q310 is present. Integrated circuit Q310 is wired as a flip-flop so that the generator can only be locked out after the level detector has changed states and the integrator is approaching zero volts. Either signal at the input to the integrated circuit Q310 (pins 1 and 2) can override the reset signal and provide for continuous running as when relay K302 is actuated or when gated through pin 1. Any command through the trigger input comparator is coupled through capacitor C303 and provides a short pulse to set the flip-flop and one cycle will be generated. When K301 is actuated and the input comparator is turned on, the generator continues to run as the flip-flop is held in that state. The flip-flop is allowed to reset after this gate signal is removed. The trigger comparator is an integrated circuit comparator with positive feedback applied

5.3.0 (Continued)

through R303 to R302. Diodes D301 and D300 protect the input of the integrated circuit comparator from large voltage swings possible at the input jack of the instrument. S304 provides a manual actuation of the input comparator so that an external voltage is not always needed to trigger or gate this generator. Diodes D302 and D303 provide the necessary operating voltages for the integrated circuit. Transistor Q305 provides the necessary 5V for operation of the Q310, the integrated circuit.

The level detector is a high-speed current mode switch whose input is differential pair Q395A and Q395B. This differential pair drives differential pair Q415 and Q430. The collectors of Q415 and Q430 are clamped by diodes. The collector output signals are also buffered by complimentary emitter followers Q405, Q410 for the collector of Q415, Q420 and Q425 for the collector of Q430. With the base of Q395B held at ground or zero volts, the switch point at the base of Q395A then becomes zero volts. The output of the integrator is fed through resistor R387 and high frequency peaking capacitors 385 and 386 to the base of the input transistor Q395A. Also connected to the input of the level detector is the switching bridge composed of diodes D390A, D390B, D391 and D392. The square signal present at the output of the complimentary emitter followers Q405 and Q410 then is applied to this switching bridge which selects either a positive or negative current to be fed to the input of the level detector. This forms the positive feedback necessary for bi-stable operation of the detector. The square wave signal that is applied to this switching bridge is also applied to the switching bridge at the input of the integrator that selects either positive or negative input current for the integrator. To analyze the operation of this detector one must assume that the output of the complimentary emitter follower Q405 and Q410 was at a positive state which selects a positive current for the level detector reference, and also a positive current for the integrator input. With this input, the output of the integrator is integrating in a negative direction. As the current through R387 (the input resistor to the level detector) reaches the same value as the current being supplied by R391 and R390 to the base of the input transistor Q395A, zero volts is reached and the level detector switches states to the other state which selects a negative input current for the integrator and a negative current through the switching bridge for the input of the level detector. In order that both polarities of the square wave are available for processing in the output amplifiers, the complimentary buffers Q420 and Q425 are provided. This buffer also provides a square wave for a synchronizing output signal.

5.4.0 D TO A CONVERTOR AND CURRENT SOURCES (Refer Figure 8.2.3)

In order to provide input current for the integrator and to provide voltage control of frequency, voltage variable current sources have been utilized. Diodes D281, D282, D283 and D280 form a switching bridge that allow the currents to be switched from negative to positive at the integrator input. The negative current source is applied to the integrator input at all times and the positive current source (which is of a value of 2 x the negative current source) can be switched on and the resultant current flow to the integrator input is equal and opposite to the value of the negative current

5.4.0 (Continued)

source. Operational amplifier Q275, transistor Q280 and transistor Q295 form an operational current source whose output is the collector of Q295 and the Drain of Q280. As the input voltage to the positive input of the operational amplifier is varied, the voltage across resistor R276 is varied. The current in the source of Q280 and the emitter of Q295 changes, varying the output of the current source. When K280 ramp reset relay is energized, resistor R280 is in the circuit and the current value of the current source is increased to approximately two times the normal value. This provides for a faster reset producing the 85 to 15 ramp-reset ratio. In order to provide level shifting and proper phase inversion for the correct polarity of drive signal, operational current source Q265 and Q270 has been provided. This current source shifts the level of the 0 to 4V available out of the summing amplifier to a +15 to +11V suitable for driving the Positive Current Source. In the same manner, operational current source Q245 (in conjunction with Field Effect Transistor Q250) provides a level shift to drive the negative current source. It takes the 0 to 4V available out of the summing amplifier and converts it from -15 to -11V suitable for input of the negative current source. The negative current source is an operational current source made up of integrated circuit Q255 and Field Effect Transistor Q260. Resistor R256 and adjustment R257 provide the operating current for transistor Q260 which is the output current of the current source. In the Triangle mode of operation, relay K260 is energized and resistor R260 and adjustment R261 are connected, increasing the value of current to maintain a symmetrical relationship for the triangle of 50% to 50%. Also being driven from the level shifted voltage generated by operational current source Q265 and transistor Q270 is the Lock-out current source which is comprised of integrated circuit Q285 and transistor Q290. This current source is used to supply a current to the lock-out diodes that is equal and opposite to the integrator input, thereby sinking all integrator input current and causing it to remain in a lock-out condition. In the Triangle mode of operation, relay K290 is energized and the value of the current output is controlled by parallel combination of resistor R293 (and its adjustment R292) and resistor R290 (and its adjustment R291).

Operational amplifier Q230 has been utilized as a summing amplifier to accept either signal from the D to A convertors or an external VCF input signal to drive the level shifting current sources. Relays K240, K241, K242 and K243 are used to provide a vernier adjustment for each decade range involving a different integrating capacitor. These relays switch in a very fine adjustment of the gain of the summing amplifier for each decade range. Balance adjustment R230 and its divider R231 through R233 is used to provide a balance for the offset voltage inherent in the integrated circuit operational amplifier. Frequency vernier adjustment R214 is also an input through summing resistor R213.

In order that no portion of the D to A convertor would have to operate at very low current level, it has been broken down into two sections with output weightings one decade apart. Operational amplifier Q205 has the highest weighting which is summed into the summing amplifier through R212. Operating at 1/10th the weighting is operational amplifier Q215 which is fed to the summing amplifier through resistor

5.4.0 (Continued)

R222. As each of the D to A convertor relays K185 and K203 is closed or opened, the output of the summing amplifier can be varied over its entire range with three digit resolution. Resistor R209 and adjustment R210 is used to provide frequency calibration. Resistor R219 and its adjustment R220 is also used to provide calibration at the low frequency end of the multiplier.

5.5.0 DECADE FREQUENCY CONTROL CIRCUIT (Refer figure 8.2.4)

The decade frequency control circuitry consists of the logic interface connections plus suitable decoding to convert a four-input BCD signal to eight lines for controlling the relays discussed previously in the generator loop circuitry. These relays control the current-sharing networks on the input of the integrator and the feedback capacitors for the integrator. The interface circuitry for the four external inputs that control the frequency decade consist of a NPN transistor used as a saturated switch and a diode switching bridge that supplies base current to the NPN transistor. Transistors Q525 through Q540 are the four saturated switches that comprise the four input BCD decade frequency control. The two diodes in series with the base lead of the transistor, for example diodes D526 and D525, provide noise immunity by increasing the amount of voltage required to saturate the NPN transistor. The two diodes D525 and D526, along with the base emitter drop of the transistor (Q525), raise the voltage required at the junction of the bias resistor R526 and the two series base diodes D525 and D526 to a potential of approximately 2.1V. At the input, such as pin 40, any voltage greater than +1.4V begins to reverse bias the input diode (D528) and the current flowing through it becomes 0 and all the current supplied by the bias resistor (R526) begins to flow through diodes D525 and D526, turning on transistor Q525. The same control over Q525 is exhibited by input diode D527. This diode is connected to the remote inhibit bus which holds the potential at the bias resistor and the transistor input point to less than .7V which does not allow the transistors to saturate. This effectively inhibits the action of all the remote inputs; therefore, it is dubbed remote inhibit bus. In the local control mode in the Model 605 only, the remote inhibit bus is held in a low state which deactivates all the external inputs and the transistors remain in an OFF condition. This allows the voltage at the collector load of the transistors to rise to the value of the positive supply voltage, providing a "one" input for integrated circuit Q550. Integrated circuit Q550 provides an "OR" function so that remote control in the Model 605 can be accomplished. The outputs of the four gates providing the four "OR" functions are fed to integrated circuit Q555. This integrated circuit provides a decimal output for a binary coded decimal input consisting of four inputs. Lamps I550 through I552 provide an automatic decimal point indication that allows direct reading of frequency from the front panel of the Model 605. The switch controlling these lamps is ganged with the decade frequency control switch. The bottom four ranges of the generator (the 1 millihertz to 1Hz range) share the same timing capacitor (the 10 μ fd capacitor) and utilize the current sharing networks to control the decade frequency. Therefore, these four lower signals are grouped together and fed to integrated circuit Q560 which controls the decoding in a manner that maintains the 10 μ fd capacitor connection while utilizing the current sharing networks for the different inputs

5.5.0 (Continued)

involved with the bottom four ranges. Integrated circuit Q565A, B and C control the current sharing network that utilizes the 2.15K resistor. Integrated circuits Q565D and Q570A and B control the current sharing network utilizing the 24.3K resistor. Integrated circuits Q575A and Q575D actuate the 10 μ fd trim relay which enables the variable resistor in the VCF summing amplifier. Q575B and Q575C activate the 10 μ fd relay. Q575A through D also provide a switching function for the CAL NORM switch. This switch defeats the 10 μ fd capacitor connection and the trim relay connection and instead actuates .01 μ fd relay and .01 μ fd trim relay so that timing of the lower frequency ranges of the instrument can be done at a higher frequency. Integrated circuit Q560A output signal actuates the short to summing junction relay, that is K320, which defeats all current sharing networks and allows full input current from the current sources to be applied to the integrator. The inverse of this signal, that is the 221 Ω relay, is actuated by integrated circuits Q570C and Q570D which inverts signal from Q560A. Integrated circuit Q585A and B provide phase inversion necessary to drive integrated circuits Q580B and C, Q590B and C for actuation of the 1 μ fd relay and the .1 μ fd relay. Also activated at the same time is integrated circuit Q580A, Q580D, Q590A and Q590D. These integrated circuits control the trim relays associated with the timing capacitors relays. Q585D provides a phase inversion necessary for operation of Q595B, Q595D while at the same time providing for the actuation of the .01 μ fd relay when the CAL NORM switch has been switched to the CAL position. The output of an integrated circuit Q595B and Q595C directly drives the .01 μ fd relay K440. Q595A and Q595D are parallel to drive the .01 μ fd trim relay. Activation of the 910pf relay is accomplished by integrated circuits Q600B and Q600C which are operated in parallel and driven from integrated circuit Q585C which inverts the signal.

5.6.0 FREQUENCY MULTIPLIER CONTROL CIRCUIT (Refer figure 8 .2.5)

In order to activate the relays associated with D to A convertor used to drive the voltage variable current sources, the interface networks consisting of the saturated transistors as shown in schematic diagram are utilized. Twelve transistors are provided to activate the twelve relays in the D to A convertor. These transistors receive their base bias current from the bias resistors such as R460. Diodes D462 and D461 are used to provide noise immunity by boosting the input voltage required to saturate the transistor to approximately 2.1V. Diodes such as D190 connected across the relay coils prevent over-voltage from appearing at the collector of the transistors due to the reactive kickback in the relay. Input diodes D463 and D464 provide input capabilities for either the remote inhibit bus or the external controlling input. As the remote inhibit bus is held at a low state, the current supplied by the base current supply resistor is shunted through diodes such as D463. This does not allow the voltage at the anode of D462 to rise to 2.1V and does not allow the transistor to be activated. When the remote inhibit bus is in a positive state or in a remote condition, the external input signal, such as through diode D466, then has complete control over the transistor switch. When the remote inhibit bus is held low, such as in a local control mode, then the relay is allowed to be actuated through diodes such as D460 to the front panel controls such as S460.

5.7.0 AMPLIFIER AND INVERTING AMPLIFIER CIRCUITS (Refer figure 8.2.6)

The amplifier and inverting amplifier circuitry consists of two high-performance wide-band operational amplifiers. One is used to provide summing and gain conditioning for the sine waveform generated by diode bridge network, the triangle waveform generated from the integrator output, and the square waveforms generated from the level detector outputs. The inputs to the amplifier are selected by function selector circuitry. The output from the integrator, being a constant amplitude due to the fact that it is controlled by the level detector, can be processed directly through a simple summing network to the operational amplifier. The triangle also is fed to a series of four diode bridges which are arranged so that they provide equal break points along the triangular waveform creating a sinusoidal function of very low distortion with an output of the proper amplitude necessary for conditioning in the amplifier circuitry. As the input voltage is raised to any one of these diode bridges, the output current from that same bridge begins to raise until it reaches the maximum value of current supplied by the resistor potentiometer combination and then it becomes a constant current source. Each bridge is turned on at a successively higher level and, therefore, provides a peak value of the combination of all four bridges for an output current at the peak of the triangle. The square waves from the level detector are processed through input relays and a switching bridge which provide a constant output current level. The complimentary emitter follower buffer circuit consisting of Q1200 and Q1205 provides a continuously monitored output of the triangular wave generated at the integrator. The output of this buffer circuit is applied directly to the rear output connector through the output resistor R1208. The sine offset relay is used to provide a current equal and opposite to the offset generated at the integrator output when the generator is operated in a 90 degree sine output mode. The offset relay K700 is used to provide the fixed DC offset when the offset control is actuated. Also actuated at the same time the offset control is actuated is relay K755 which parallels the operational amplifier feedback resistor with a resistor of an equal amount, reducing the gain to one-half the original value. The output of this amplifier circuitry is applied directly to the input of the inverting amplifier which is operated at a gain of 1. Being an operational amplifier, it provides 180 degree phase inversion giving then two phases for processing in the amplitude selector. These two operational amplifiers are nearly identical with two signal paths in each amplifier. One signal path covers frequencies from DC to approximately 100KHz and the other signal path processes frequencies above 100KHz. The input circuitry for the low frequency path is a differential pair consisting of Q710, a matched pair of silicon transistors. Resistive divider made up of R715 to R719 is used to compensate for the differences in the base emitter drops of these input transistors. The output of this differential pair and their collector load resistors R711 and R712 are applied to differential pair Q715 and Q725. Single-ended output appearing at the collector of Q715 of this differential pair is applied to a differential mixer made up of Q730 and Q740. This differential mixer mixes the low frequency signal path and the high frequency signal path. The input circuitry for the high frequency signal path flows through Junction Field Effect Transistor Q720 through capacitor C740 to the other input of the differential mixer Q740. The collector signal Q730 is fed to inverter transistor Q735 so that a complimentary signal of the same phase as the output of

5.7.0 (Continued)

collector Q740 is available for processing in the complimentary emitter follower buffer consisting of Q745 and Q750. Diodes D735 and D740, along with resistor R742, provide the quiescent bias voltages necessary for operation of the complimentary buffer Q745 and Q750. Diodes D745 and D750 provide short circuit protection in the event that the output of this amplifier were accidentally short circuited. The inverting amplifier operates in the same manner as the amplifier previously described and its circuitry is identical with the exception that the feedback components and the input resistors are of different value to provide the necessary gain of one. The output of the inverting amplifier is also fed to a phase selector called the invert relay so that either phase can be fed to the amplitude selector.

5.8.0 FUNCTION CONTROL CIRCUITRY (Refer figure 8.2.7)

Function control circuitry, as shown, consists of four different inputs and their input interface circuitry and the decoding logic necessary to operate the appropriate relays in the generator circuitry. Q610, Q995, Q975 and Q980 are the saturated switches and for a description of their operation refer to Section 5.6.0. The outputs of these saturated switches are fed to the decoding circuitry directly. Integrated circuit Q615D is used to invert the signal from the saturated switch Q610. The output of Q615D is used to drive the parallel combination of the integrated circuits Q620A and Q620D. This output in turn drives the relay K291. The parallel combination of integrated circuits Q615B and Q615C directly drives relay K260. The parallel combination of integrated circuits Q620 and Q620C directly drives relay K290. The logic involved with these three relays is such that the symmetry in the generator loop circuitry can be set for a 50% to 50% ratio or an 85% to 15% ratio. For local control in Model 605, switch decks S610D and S610E control this symmetry on the ramp functions and the pulse functions so that the ratio is 85-15 and all other functions so that the ratio is 50-50. Integrated circuits Q1005A and Q1005D receive their signals from a saturated switch Q995 and from the local control switch deck S610E in the Model 605. The outputs of these integrated circuits are used to directly drive the relays in the generator loop circuitry that create the 90 degree start point in the waveform as compared to the 0 degree start point. Integrated circuits Q1005B and Q1005C are used to provide the operating potentials for relay K677 which provides the offset necessary in the sine shaping network to provide the Haversine waveform, when the generator is programmed for a start level of 90 degrees as compared to the 0 degrees start level. Integrated circuits I015A and I015D receive the outputs of the saturated switch Q975. Integrated circuits Q1015 and Q1015C receive the outputs from saturated switch Q980. These integrated circuits also can receive the signals from the local control switch deck S610A and S610C. The outputs of these integrated circuits are decoded in a manner so as to provide the necessary switching of the relays to connect the sine shaper to the amplifier circuitry or the positive or negative square to the amplifier circuitry or the triangle, etc. Integrated circuit I025A is used to drive relay K695. Integrated circuit I025B is used to drive relay K702. This relay is used to provide offset current in the amplifier circuitry so that the ramp waveform, when processed at 0 degrees start level, can be used as a bipolar signal. Relay K695 is used to apply the output of the sine shaper bridges

5.8.0 (Continued)

to the amplifier circuitry. Integrated circuit Q1030B is used to drive the relay K675 from the outputs of both Q1015C and Q1015B. Relay K675 is used to apply the triangular signal from the integrator to the input of the sine shaping bridges. Integrated circuit Q1030A is used to drive relay K705 when activated from a signal from Q1015A and Q1015C. Relay K705 provides a triangular waveform for processing in the amplifier circuit. Integrated circuit Q1025B and Q1025C are parallel combination used to operate relay K935. Relay K935 supplies the inverting square to the square switching bridge. Integrated circuit Q1020A and Q1020D are parallel combination that operates K936. Relay K936 is used to provide the positive square to the square wave switching bridge. Integrated circuits Q1020B and Q1020C drives relay K937 which is used to apply the output of the square switching bridge to the input of the amplifier circuitry.

5.9.0 FUNCTION AND TRIGGER MODE CIRCUITRY (Refer figure 8.2.8)

The function and trigger mode circuitry, as shown in the schematic diagram, consists of four separate inputs and their saturated switches and necessary decoding logic to decode these signals to drive the phase control, offset control, and trigger mode control. Transistors Q985, Q990, Q630 and Q645 are the saturated switches used to process the incoming signals from the external programming source. The outputs of these saturated switches are used directly as inputs to the integrated circuits used to decode the input signal. Integrated circuit Q1000A and Q1000D are parallel combination used to drive relay K760. They also provide the necessary input for the local control of the Model 605 of the PHASE NORMAL INVERT switch. Integrated circuit Q1000D and Q1000C are parallel combination used to drive relay K761. These two relays are used to provide either one signal from the amplifier circuit to be processed in the amplitude selector or the output of the inverting amplifier to be processed in the amplitude selector. Integrated circuit Q1010B and Q1010C is a parallel combination used to drive relay K700. Integrated circuit Q1010B and C accepts the signal from saturated switch Q990 and from the local control of the Model 605 OFFSET switch. Integrated circuit Q1010A and Q1010D are used to operate relay K755. These two relays provide for selecting the offset signal applied to the amplifier circuitry through fixed bias resistor and also for reducing the gain of the amplifier circuitry by paralleling the feedback resistor of the operational amplifier. Integrated circuit Q635B accepts the signal from saturated switch Q630 or from the TRIGGER mode switch on the front panel of Model 605. The output of this integrated circuit is fed to integrated circuit Q640A and Q640B which operates relay K302. Relay K302 is a continuous run relay on the trigger circuitry. Integrated circuits Q635C and Q635D decode the two inputs and are capable of operating the optional relay K300. This relay is used to provide an inhibit signal to inhibit any trigger from operating the generator when activated. Integrated circuit Q635A accepts the signal from saturated switch Q645 or from the local control TRIGGER mode switch S630B. The output of this integrated circuit is fed to parallel combination of Q640C and Q640D which drives relay K301. Relay K301 is used to provide for either AC or DC coupling of the trigger comparator circuit so that a gated or a triggered mode of operation is available.

5.10.0 OUTPUT AMPLIFIER CIRCUITRY (Refer figure 8 .2.9)

Output amplifier circuitry, as shown in the schematic diagram, consists of a wide-band high-performance operational amplifier capable of supplying large amounts of output current. The amplitude selector, as shown, consists of a series of input resistors to this operational amplifier that can be switched on and off providing a control with twelve binary bits. Relays K820 thru K842 operate as switches that can either apply the signal from the phase selector relays directly to the input resistors or leave the circuitry open so that no signal is applied to that resistor. In order that accuracy can be obtained, resistors of the most significant values are provided with an adjustment for gain trimming. Also available as an input to this output amplifier is the analog DC offset programming signal from the rear panel connection. This input is applied to the summing junction of the operational amplifier thru resistor R844. The operational amplifier consists of two signal paths, one covering the frequencies from DC to approximately 100KHz and the other processing the signals from 100KHz and above. These two signals are mixed together in a differential mixer and applied to the output buffers and from there to the decade voltage control circuitry. Dual Junction Field Effect Transistor Q850 accepts the DC to 100KHz input signals and applies them to differential pair Q860 and Q865. The output of this differential pair is taken in a single-ended manner and fed to one input of the differential mixer Q875. The frequencies above 100KHz are applied to the differential mixer through input transistor Q870 which is a high frequency Junction Field Effect Transistor. The output of differential mixer Q875 is fed to the inverter driver Q880. This transistor inverts a signal and increases the power level to a sufficient level to drive the output buffers. The output of Q885 which is one transistor of the differential mixer pair is applied directly to the output buffers. Quiescent operating bias voltages are developed thru the diode resistor combination of D880, D885 and R887. Transistors Q890 thru Q905 form a complimentary buffer circuit with each compliment being a parallel combination of two transistors. These transistors have heat sinks to maintain safe operation at the high power levels involved with the output circuitry of the generator. The feedback resistor from the output to the summing junction is R845 which is paralleled by a compensation capacitor combination C845 and C846. The decade voltage selector consists of a series of relays used to operate 20db pads so that the signal can be attenuated in ratios of 10:1 for each decade of output voltage selection. The parallel combination of R906, R907 and R908 provides the 50 Ω output impedance for the output amplifier circuitry. All attenuator sections in the decade voltage selector provide the output impedance of 50 Ω also. Therefore, it is necessary that the generator circuit also be operated into 50 Ω to maintain amplitude accuracy, waveform quality, etc.

5.11.0 OUTPUT AMPLIFIER CONTROL CIRCUITRY (Refer figure 8 .2.10)

The output amplifier control circuitry consists of a series of saturated switches that accept the external input commands and actuate the relays involved with the amplitude selector circuitry. These saturated switches operate in the same manner as previously discussed for input signal conditioning. The extra diode as DI040, DI045, etc., provide for a local control in the Model 605. This allows the switch to directly operate the relay when the saturated switch has been inactivated by the remote inhibit bus.

5.12.0 OUTPUT ATTENUATOR CONTROL CIRCUITRY (Refer figure 8.2.II)

The output attenuator control circuitry consists of two saturated switches for accepting the external input signals. The outputs of these saturated switches are fed to decoding logic so that four different ranges can be accommodated with only two inputs from an external source. The logic circuitry also provides for operation in a local control in the Model 605. Integrated circuits Q955A and B are parallel combination that accepts the input from Q945 and applies it directly to operate relay K916. Integrated circuit Q955C inverts the signal from saturated switch Q945 and applies it directly to integrated circuit Q960A and Q960D whose output is paralleled to operate relay K910. Integrated circuit Q955D is used to invert the signal from saturated switch Q950. The output of saturated switch Q950 is applied directly to the input of integrated circuit Q965B and Q965C. This integrated circuit directly drives relay K915. Q970A and D are paralleled for operation of K921. Q970B and C are also paralleled for operation of K925. Switch deck S955D is used to operate the automatic decimal point indicating lamps I955 and I957. These lamps allow the front panel controls to be read directly in output voltage.

SECTION 6

CALIBRATION PROCEDURE

6.1.0 EQUIPMENT REQUIRED

The following test equipment or suitable equivalents of known accuracy are required for complete calibration of the Models 605 and 606 Programmable Waveform Generators.

Adjustable line voltage transformer, Superior Powerstat or equivalent
 Differential or digital voltmeter capable of resolving 1mv and 15V
 Oscilloscope, D.C. through at least 50MHz bandwidth
 Differential plug-in capable of resolving 1mv in 15V
 Frequency and time interval counter
 Distortion analyzer, Hewlett Packard 333A

6.2.0 INITIAL CONTROL SETTINGS

POWER switch	ON
FREQUENCY dials	800Hz
FUNCTION	TRIANGLE
VOLTAGE	8.00V
TRIGGER mode	RUN
PHASE	NORMAL
OFFSET	OFF
DELTA FREQUENCY (Model 605 Only)	CAL

6.3.0 CALIBRATION (Refer figure 6.3.1 and 6.3.2)

After a 30-minute warm-up time, the instrument is prepared for calibration.

1. Connect DVM or Differential Voltmeter to 22V test point and adjust 22V adjust for $22.0V \pm 10mv$.
2. Connect DVM to -22V test point and adjust -22V adjust for $22.0V \pm 10mv$.
3. Connect DVM to +15V test point and adjust the +15V adjust for $+15.0V \pm 2mv$.
4. Connect DVM to -15V test point and adjust the -15V adjust for $-15.0V \pm 2mv$.
5. **CAUTION:** The following adjustment is necessary only in cases of extreme mal-adjustment and/or catastrophic failure. The crowbar adjustment requires that the logic power supply +5V be over-voltaged to 5.5V and possible damage to the integrated circuits. Extreme caution must be exercised. To adjust the crowbar, you must adjust the +5V adjust to a voltage of maximum or not greater than 5.5V. Upon achieving this, advance crowbar adjustment until the output waveform from the instrument ceases. This indicates that the 5V power supply is crowbarred and you may now return the 5V adjustment to midscale. Turn instrument power switch OFF and then return to ON again. Instrument output waveform should be restored. It is necessary to readjust the +5V power supply upon completion of this test at any time.

6.3.0 (Continued)

6. Connect DVM to TP117 and adjust the +5V adjust for $5.0V \pm 10mv$.
7. Using adjustable line transformer, vary line voltage between 105V and 125V AC and probe each power supply in turn, checking regulation. $\pm 22V$ supplies should regulate within 20mv. $\pm 15V$ supplies should regulate within 2mv. +5V supply should regulate within 10mv.
8. Connect oscilloscope with differential plug-in to integrator output TP386. Monitor comparison voltage on the differential plug-in with Digital Voltmeter so that accuracy can be maintained to within 1mv. Adjust positive peak adjust for positive triangle peak of $5.00V \pm 2mv$. Adjust negative peak adjust for negative peak of triangle to be $5.00V \pm 2mv$.
9. Using DVM on most sensitive range, probe test point LSB. Adjust LSB balance adjust for $0V \pm .1mv$. NOTE: Use TP243 as ground point during these measurements.
10. Reset frequency dial to 000.Hz and connect DVM to test point MSB. Adjust MSB balance adjustment for $0.00V \pm .1mv$.
11. Connect DVM to rear side of R267 and adjust VCF balance control for a voltage reading of $0.00 \pm .2mv$.
12. Readjust frequency for a reading of 001Hz and note DVM reading as connected in previous adjustment. Connect DVM across R251 and adjust minus drive balance for the same voltage reading as obtained in the noted adjustment. Connect DVM across R270 and adjust plus drive balance adjust for same voltage reading as obtained in previous test.
13. Reprogram generator for frequency to 00XHz. Take reading across R270. Connect DVM across R276 and adjust positive current balance for new reading. Connect DVM across the combination of R256 and potentiometer R257. Adjust the negative current balance adjust for the same reading obtained in the positive current balance adjust.
14. Program generator for a positive pulse output. Connect frequency counter to the generator output and adjust the time interval of the output pulse by manipulating the generator frequency controls until a reading of $150.0\mu s$ is achieved. Switch counter from reading time interval to reading period of the pulse and adjust ramp time adjust for a reading of $1000\mu s$.
15. Program generator for a positive square output and set counter to read time interval. Adjust the symmetry adjust until time symmetry can be obtained by reading both time intervals of the square signal.
16. Program generator for an 80.0KHz squarewave output signal. Connect counter to squarewave and read frequency. Adjust the 80F adjustment for 80.0KHz output

6.3.0 (Continued)

signal. Reprogram generator for 40.0KHz and adjust the 40F adjustment for 40.0KHz. Reprogram generator for 20.0KHz and adjust the 20F adjust for a 20.0KHz signal. Reprogram generator for 10.0KHz and adjust the 10F adjust for 10.0KHz signal. Reprogram generator for 08.KHz and adjust the 8F adjust for 8KHz output signal. Reprogram generator for 04.0KHz and adjust the 4F adjust for 4KHz output signal.

17. Reprogram generator for an 800KHz squarewave and adjust high frequency comp adjustment for 800.0KHz. Reprogram generator for a 100KHz squarewave and adjust the 80KHz adjust for 100.0KHz.
18. Reprogram generator for an 80.0KHz squarewave and readjust the 80F adjust for 80.0KHz. Readjust the 8F adjust for 8.0KHz.
19. Repeat steps 16 through 18 until a satisfactory adjustment has been achieved.
20. Reprogram generator for a frequency of 10.00KHz. Adjust the 10KHz adjust for 10.00KHz. Reprogram generator for 1000Hz. Adjust the 1000Hz adjust for 1000Hz. Reprogram generator for 100.0Hz. Adjust the 100Hz adjust for 100.0Hz. Reprogram generator for 10.00Hz and adjust the 10Hz adjust for 10.00Hz.
21. Reprogram generator for a frequency of 1000mHz. Adjust 1000mHz timing adjust for 1000mHz.
22. Adjust 10mHz symmetry adjust for a time symmetry.
23. Repeat steps 20 through 21 as needed.
24. With generator operating at 1000mHz, switch CAL NORM switch to CAL and record reading of frequency counter. Reprogram generator for a frequency of 100mHz and adjust 100mHz timing adjust for a frequency reading one decade lower than obtained in the CAL position at 1000mHz. Reprogram generator for a frequency of 10mHz and adjust frequency for one decade value lower than obtained in previous tests. Return CAL NORM switch to NORMAL.
25. Program generator for a 1000Hz triangle and monitor the output of the amplifier at R751. Adjust the balance adjust for triangle peaks to be within 2MV absolute value one another.
26. Program generator for sinewave output. Connect distortion analyzer to output and adjust sine input adjust for minimum sine distortion. Readjust distortion adjust 1, 2, 3, and 4 for minimum distortion. Interaction between adjustments may necessitate readjusting certain adjustments.
27. Program generator for an output voltage of 0.00V and adjust output amplitude balance for $0V \pm 5MV$.

6.3.0 (Continued)

28. Reprogram generator for an output voltage of 8.00V sinewave. Adjust sine peaks A and B along with the gain adjust control for an output sinewave of 8V P-P ± 2 MV. Sine peak A and sine peak B adjustments are used to control the DC component.
29. Reprogram generator for a triangular wave output signal and adjust triangle amplitude adjust for triangle output amplitude of 8.00V P-P ± 5 MV.
30. Reprogram generator for a positive square output and adjust the + square adjust and - square adjust for an output amplitude of 8.00V P-P ± 10 MV.
31. Program generator for Offset function. Adjust Offset adjust for the negative peak value to be 0V ± 10 MV and adjust the Gain/2 adjust for the positive peak to be 4.0V ± 10 MV.
32. Program generator for an inverted phase output signal. Adjust the inverting gain adjust and the inverting balance adjust for 8V P-P ± 10 MV.
33. Program generator for an output voltage of 4.00V P-P and adjust the 40 adjust for 4.00V. Program generator for 2.00V output signal. Adjust 20 adjust for 2V. Program generator for 1.00V output level. Adjust 10 adjust for 1.00V. Program generator for .8V P-P output level. Adjust 8 adjust for .8V P-P. Program generator for .4V P-P. Adjust 4 adjust for .4V P-P output level.
34. Program generator for a ramp function at 8V P-P. Switch trigger mode to Gate. adjust the Ramp Offset Adjust so that the start level is at -4.00V ± 10 MV.
35. Reprogram for free running ramp and adjust L.O. Offset adjust for the negative peak of the ramp to be -4.00V ± 10 MV.
36. Reprogram generator for a Haversine waveform and adjust the Sine Offset adjust for minimum distortion.
37. Reprogram generator for ramp output in Gate mode and adjust the Ramp L.O. adjust for -4.00V ± 10 MV at the output.
38. Reprogram for triangle output in the Gate mode and adjust the Triangle L.O. adjust for 0V ± 10 MV.
39. Reprogram frequency multiplier for 010.Hz and adjust the X100 L.O. Balance for 0V ± 10 MV.
40. Reprogram generator for 999KHz squarewave and probe the amplifier at R751 and adjust the Comp adjust for minimum ringing and overshoot.
41. Probe the Inverting Amplifier at R811 and adjust the Inv Comp adjust for minimum ringing and overshoot.

6.3.0 (Continued)

42. Monitor output waveform and adjust the Output Comp adjust for minimum overshoot and ringing while also checking for minimum deviation of sine wave output amplitude.

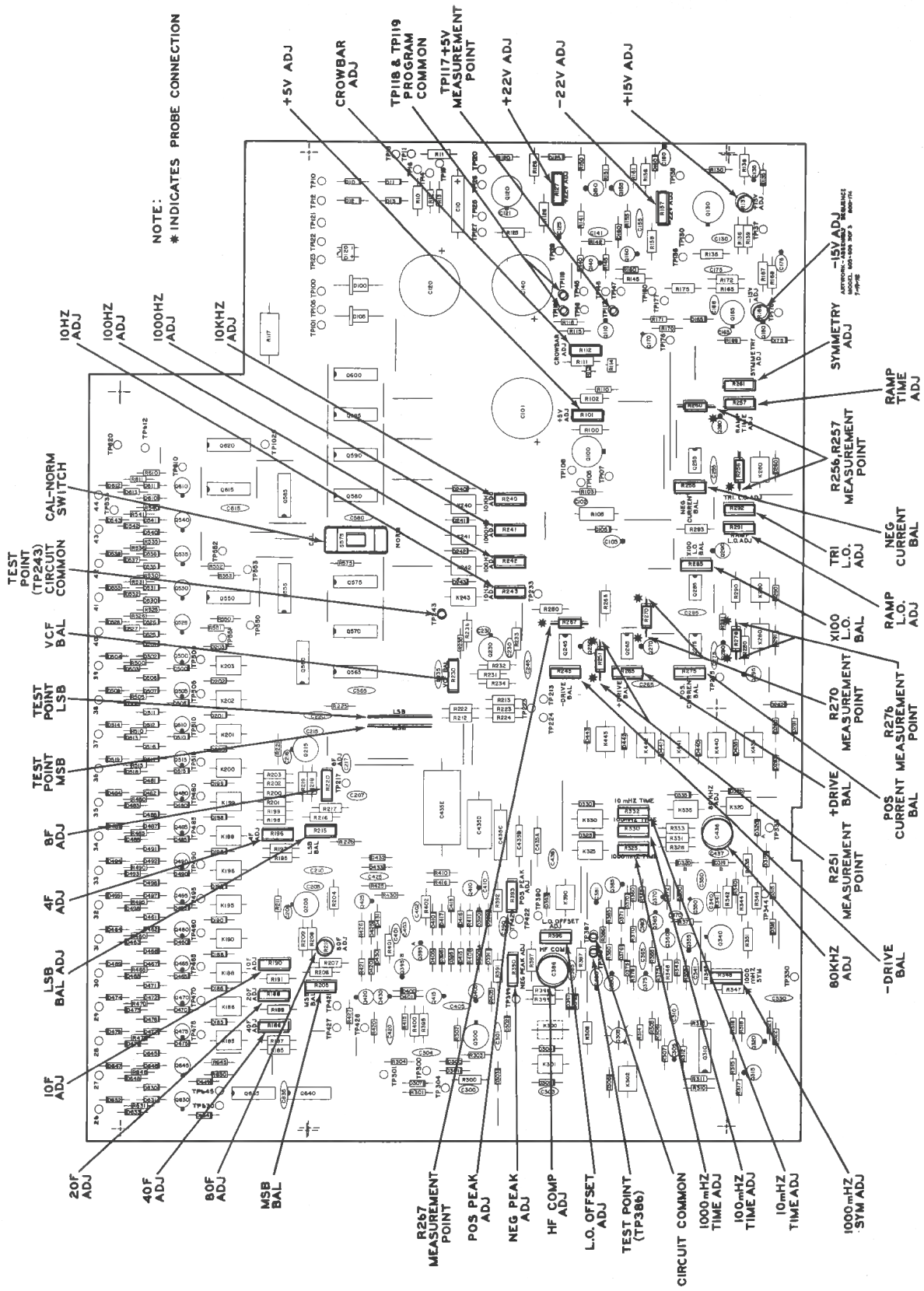


FIGURE 6.3.1 ADJUSTMENT LOCATION DETAIL

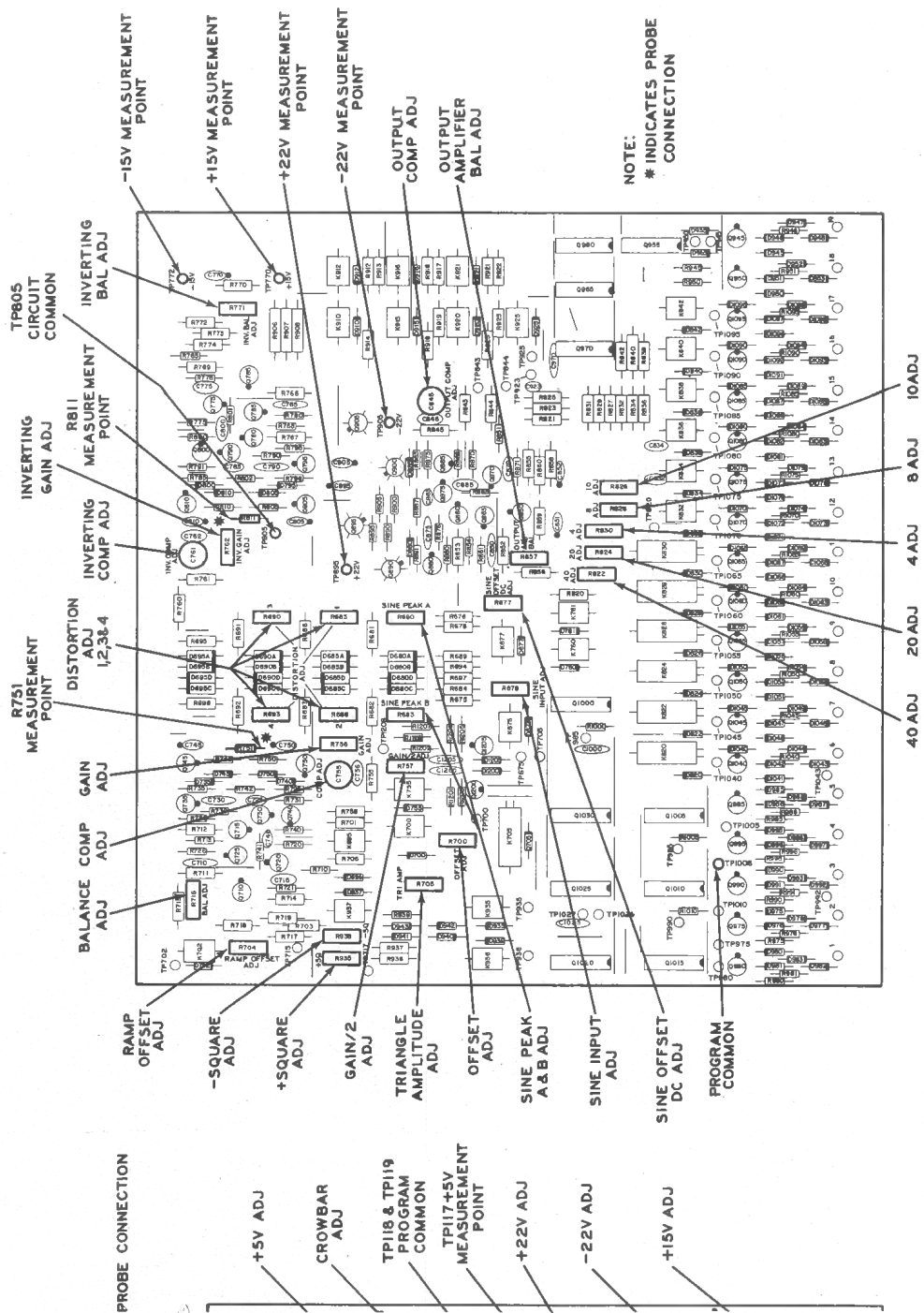


FIGURE 6.3-2 ADJUSTMENT LOCATION DETAIL

SECTION 7

PARTS LIST

SECTION 7

PARTS LIST

PART	DESCRIPTION	EXACT NO	MFG
R1207	RESISTOR, 22 OHM 1/4W 5% CARBON	3070220	1121
R1208	RESISTOR, 560 OHM 1/4W 5% CARBON	3070561	1121
S0100	SWITCH, TOGGLE SPDT	2600103	100005
S0101	SWITCH, SLIDE	2600319	10597
S0304	SWITCH, PUSHBUTTON SPDT	2600086	100005
S0460	SWITCH, BCD ROTARY	2600324	10597
S0480	SWITCH, BCD ROTARY	2600324	10597
S0500	SWITCH, BCD ROTARY	2600324	10597
S0550	SWITCH, BCD ROTARY WITH INH.	2600325	10597
S0575	SWITCH, SLIDE DPDT	2600212	76854
S0610	SWITCH, ROTARY 7 POSITION	2600326	10597
S0630	SWITCH, LEVER SP3T	2600251	10597
S0955	SWITCH, BCD ROTARY WITH INH.	2600325	10597
S0985	SWITCH, TOGGLE SPDT	2600103	100005
S0990	SWITCH, TOGGLE SPDT	2600103	100005
S1040	SWITCH, BCD ROTARY	2600324	10597
S1060	SWITCH, BCD ROTARY	2600324	10597
S1080	SWITCH, BCD ROTARY	2600324	10597
T0100	TRANSFORMER, POWER	1200040	10597

SECTION 8

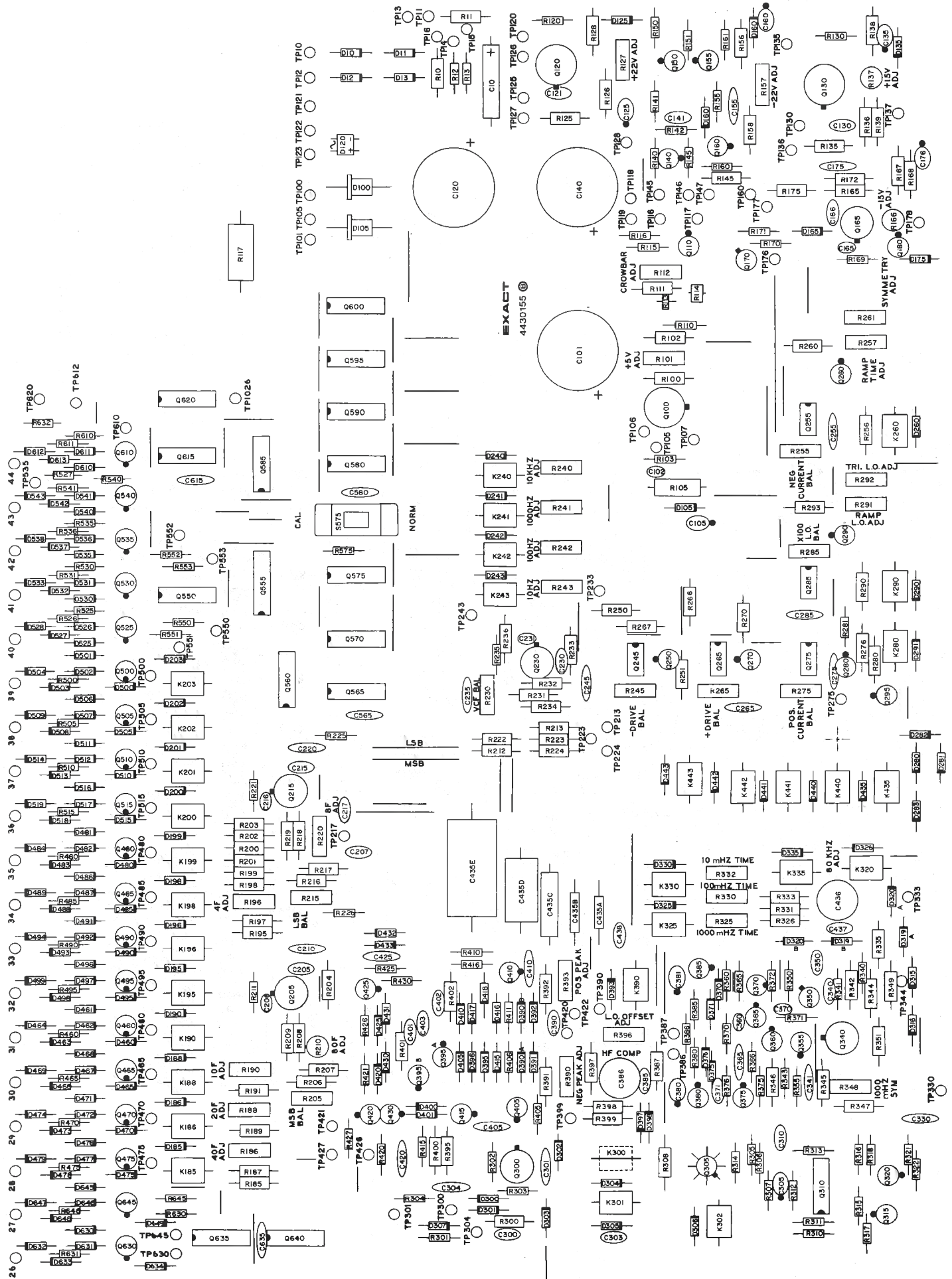
PARTS LAYOUT AND SCHEMATICS

SECTION 8

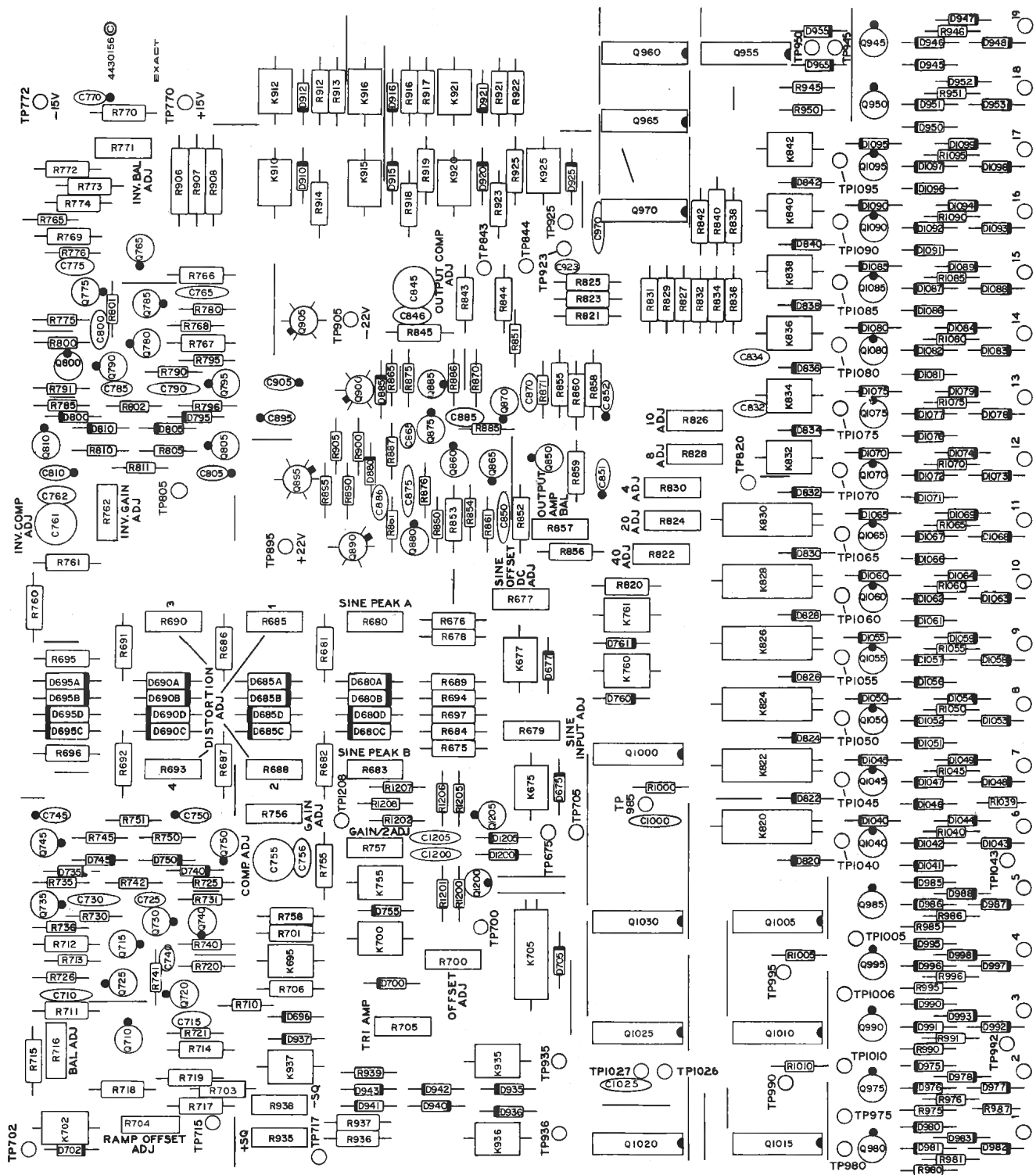
FOREWORD TO SCHEMATICS

For purposes of clarity, power supply connections to the integrated circuits used in control circuitry have been omitted. The following rules apply. All integrated circuits S/N 7400N or equivalent pin number 7 connected to programming common V_p , and pin number 14 connected to +5V. All integrated circuits S/N 7440N or equivalent (except Q310) pin number 7 connected to programming common, and pin number 14 connected to +5V. Q310 is isolated from program common and has its own power supply which is derived from +15V. All integrated circuits S/N 7442N or equivalent pin number 8 connected to programming common and pin number 16 connected to +5V.

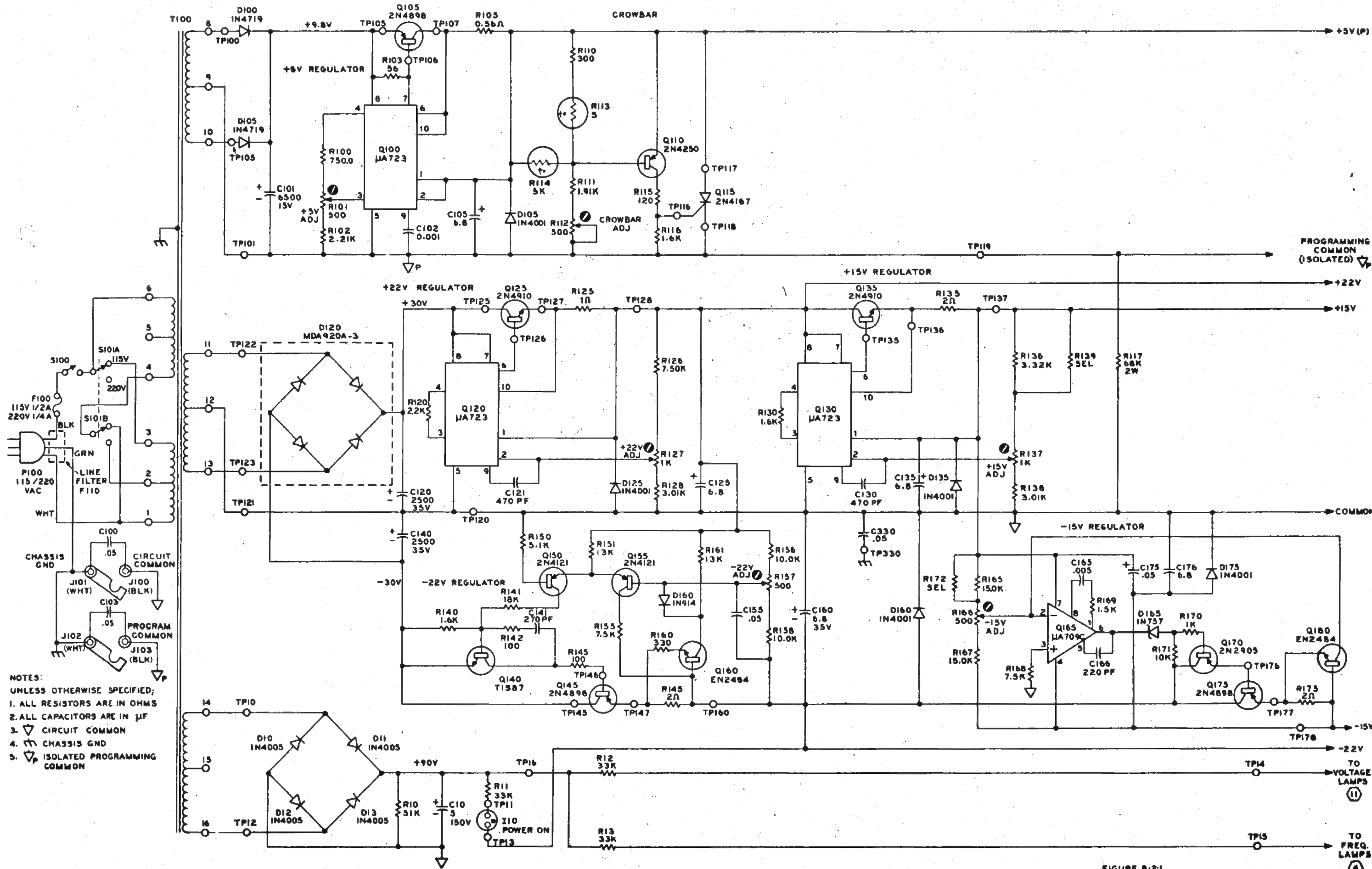
To facilitate quick reference to inter-connections from one schematic to another, a system of numbers has been utilized. For instance, the relays involved in the control circuitry have relay coils on one schematic and relay contacts on another. Each schematic carries its own identifying number located in a large hexagonal shape near the title. When a connection is referred to, a small hex encompasses the number of the schematic that contains the connection.



PARTS OVERLAY (figure 8.1.0)

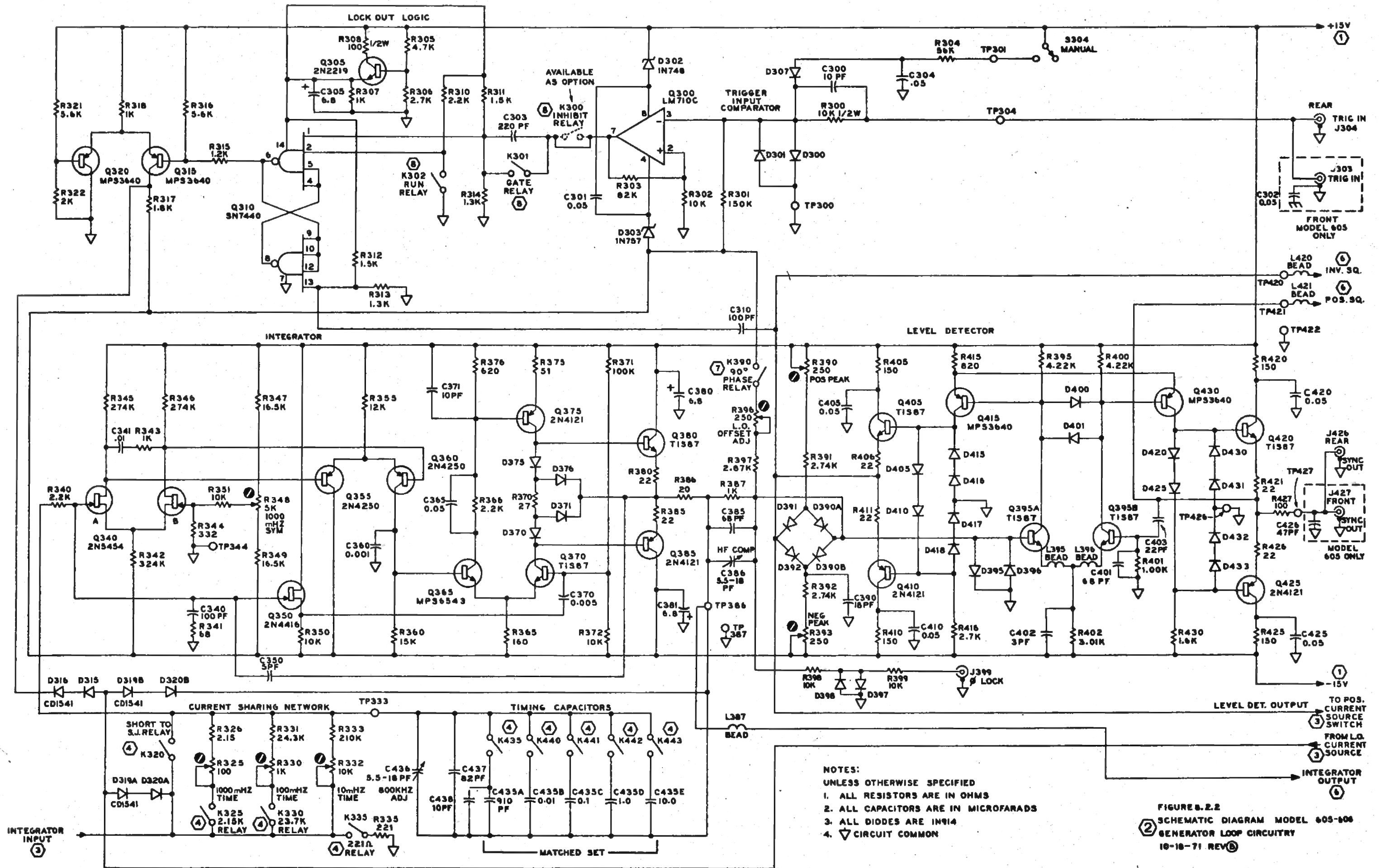


PARTS OVERLAY (figure 8.1.1)



NOTES:
 1. ALL RESISTORS ARE IN OHMS
 2. ALL CAPACITORS ARE IN μF
 3. ∇ CIRCUIT COMMON
 4. ⏏ CHASSIS GND
 5. ⏏ ISOLATED PROGRAMMING COMMON

FIGURE 8-21
 ① SCHEMATIC DIAGRAM MODEL 605-606
 POWER SUPPLY CIRCUIT
 10-18-71



NOTES:
 1. ALL RESISTORS ARE IN OHMS
 2. ALL CAPACITORS ARE IN MICROFARADS
 3. ALL DIODES ARE 1N914
 4. ▽ CIRCUIT COMMON

FIGURE 8.2.2
 SCHEMATIC DIAGRAM MODEL 605-606
 GENERATOR LOOP CIRCUITRY
 10-18-71 REV B

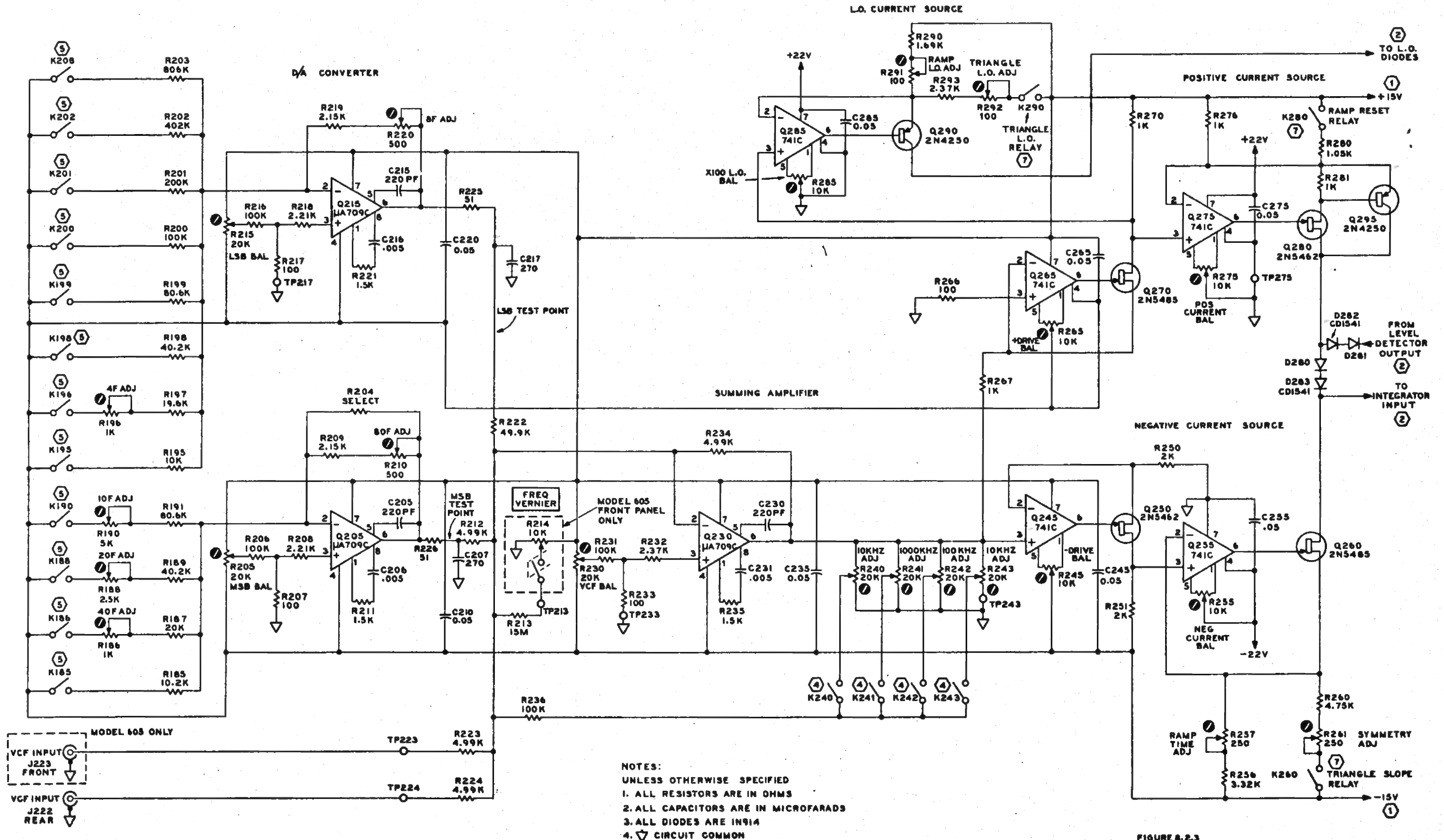
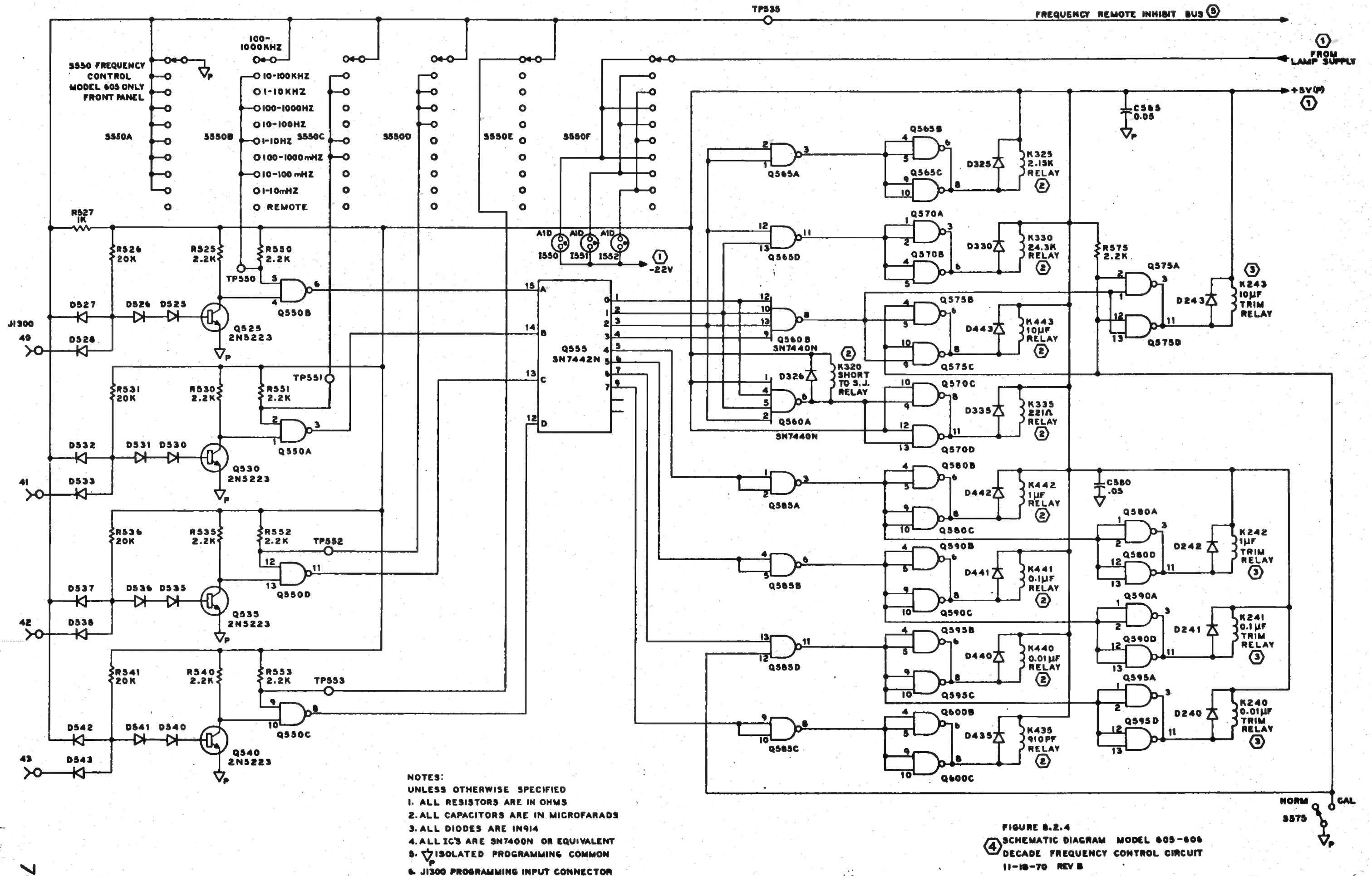
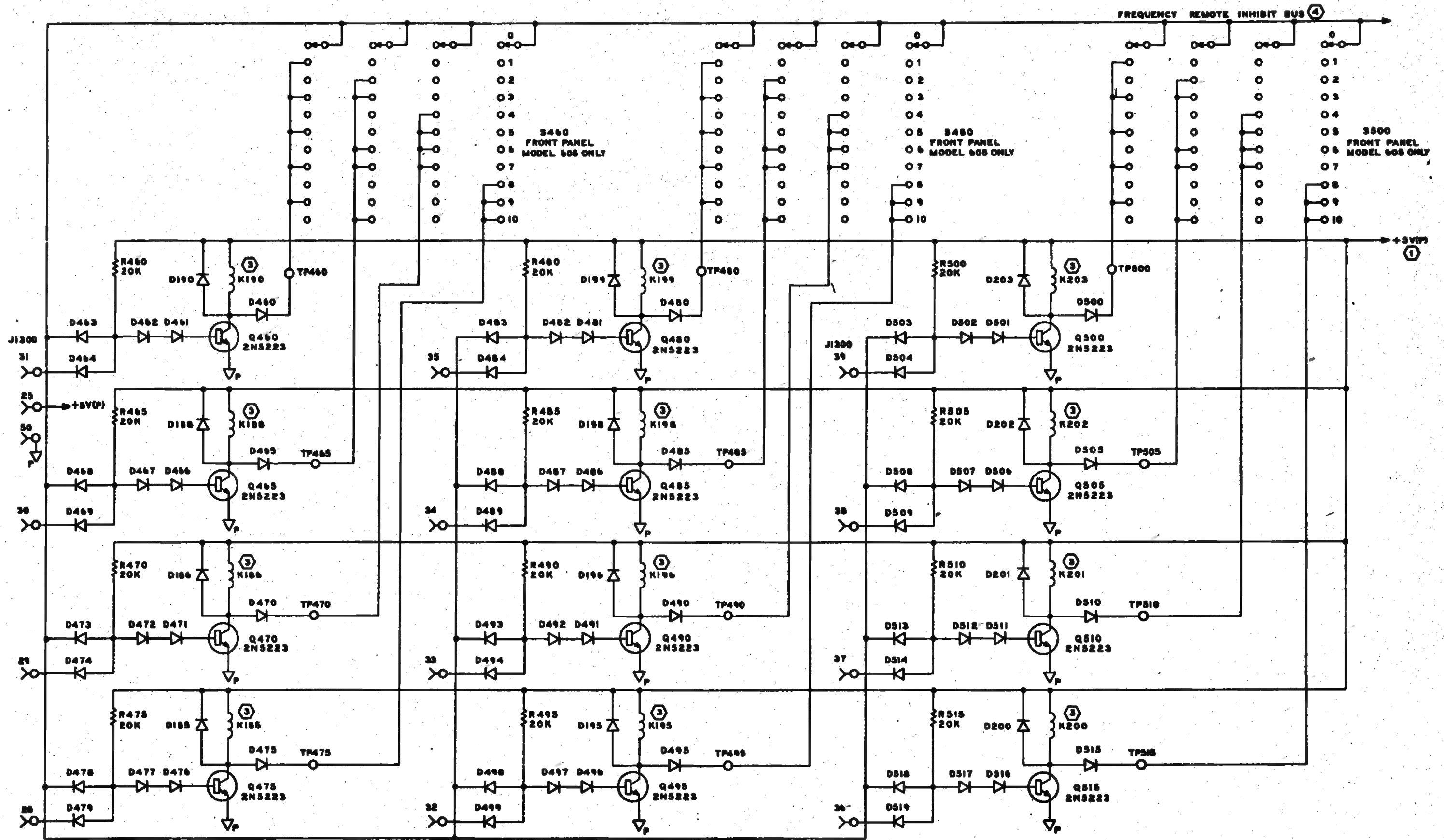


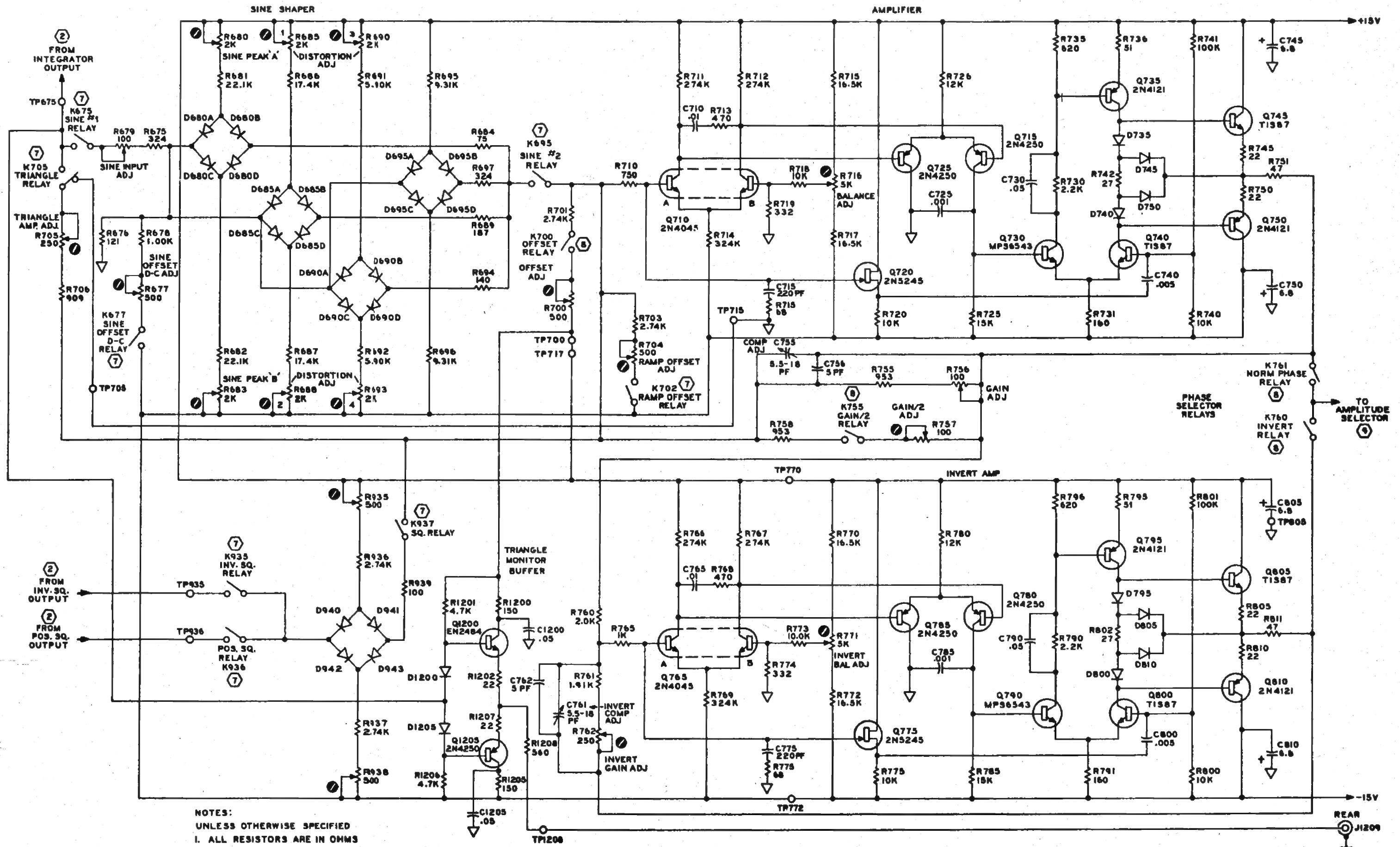
FIGURE 8.23
 SCHEMATIC DIAGRAM MODEL 605-606
 D/A CONVERTER & CURRENT SOURCES
 11-18-70





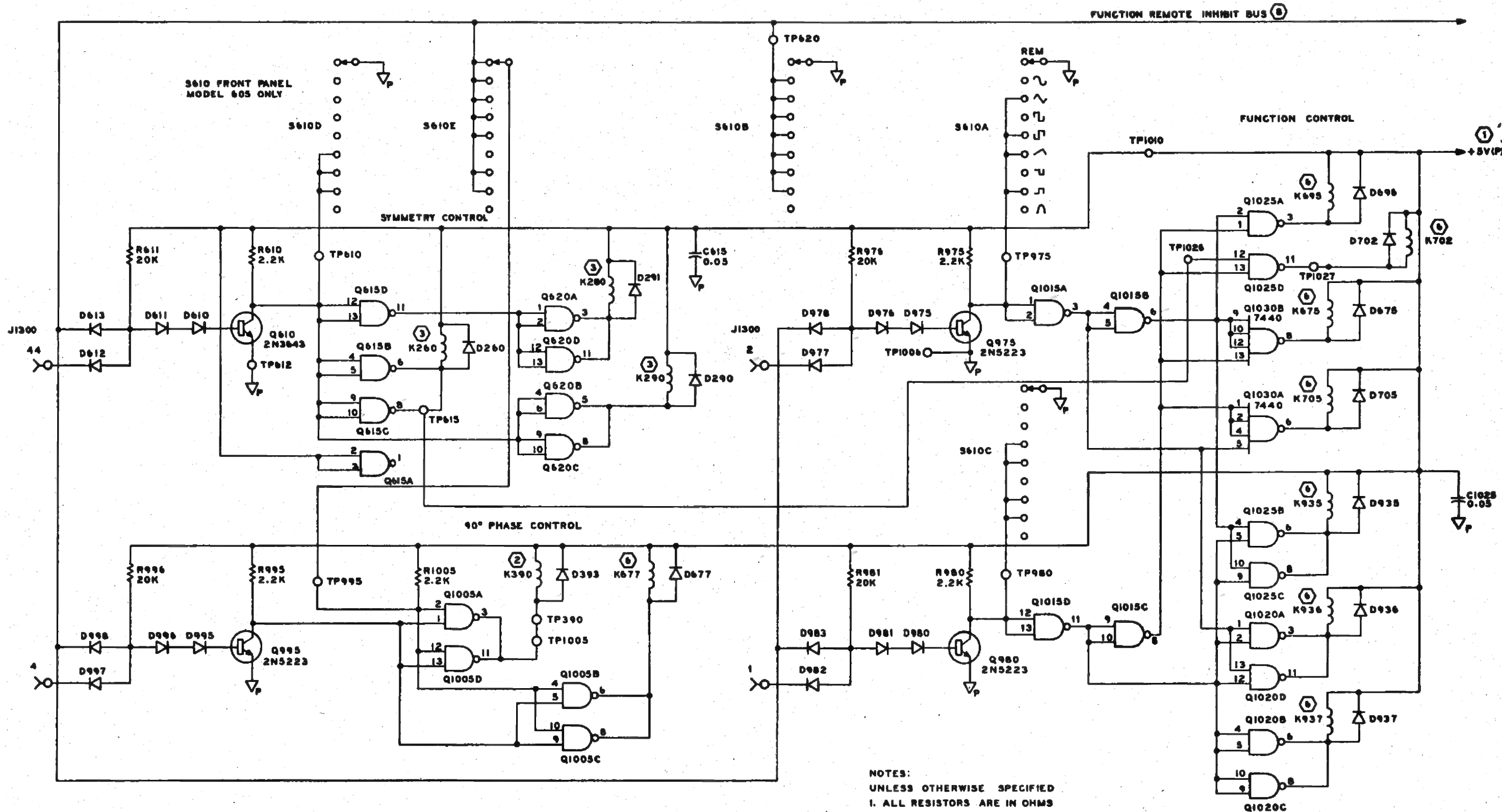
- NOTES:
 1. ALL RESISTORS ARE IN OHMS
 2. ALL CAPACITORS ARE IN MICROFARADS
 3. ALL DIODES ARE IN914
 4. ISOLATED PROGRAMMING COMMON
 5. J1300 PROGRAMMING INPUT CONNECTOR

FIGURE 8.2.5
 SCHEMATIC DIAGRAM MODEL 605-606
 FREQUENCY MULTIPLIER CONTROL CIRCUIT
 11-18-79



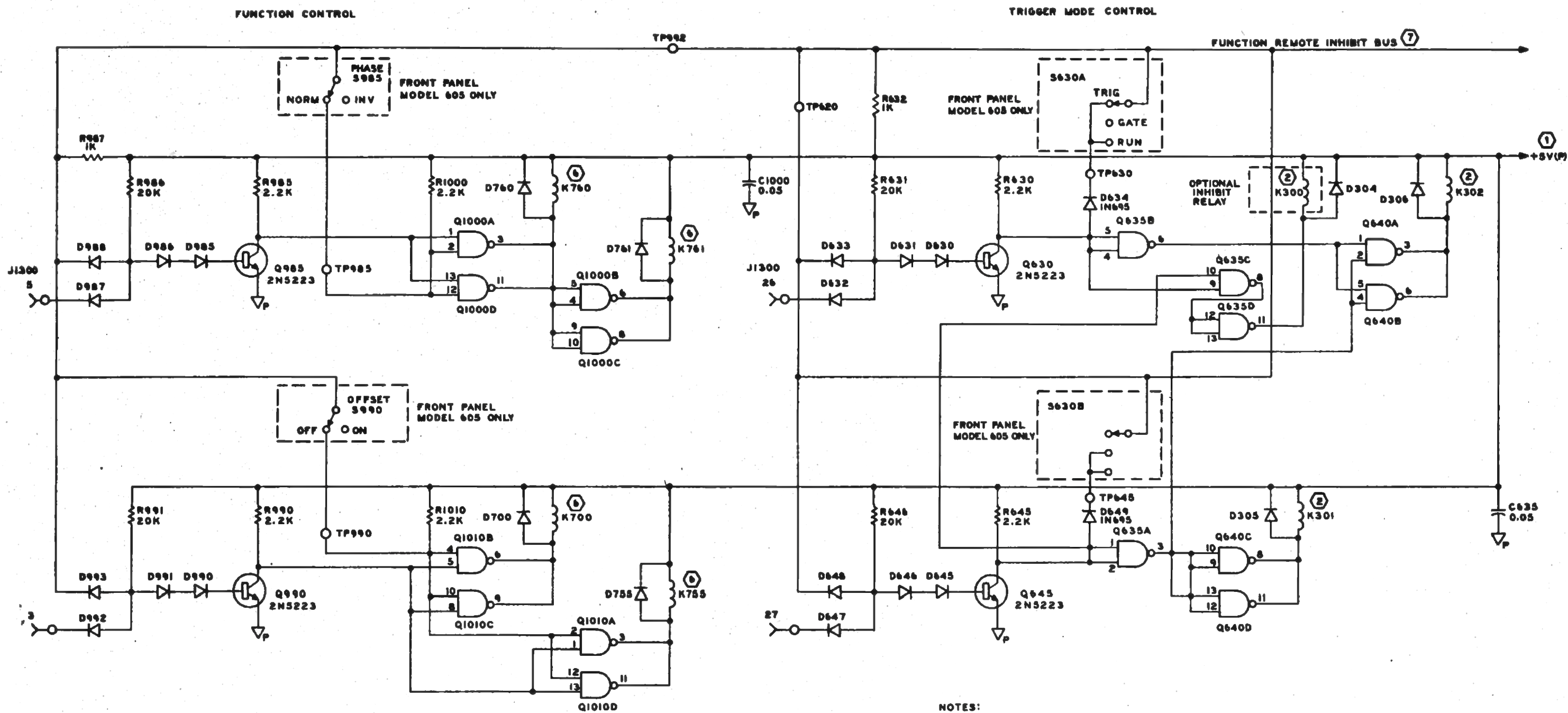
NOTES:
 UNLESS OTHERWISE SPECIFIED
 1. ALL RESISTORS ARE IN OHMS
 2. ALL CAPACITORS ARE IN μ F
 3. ALL DIODES ARE IN914
 4. ∇ CIRCUIT COMMON

FIGURE 8-26
 SCHEMATIC DIAGRAM MODEL 605-606
 AMPLIFIER AND INVERTING AMPLIFIER CIRCUITS
 11-18-76



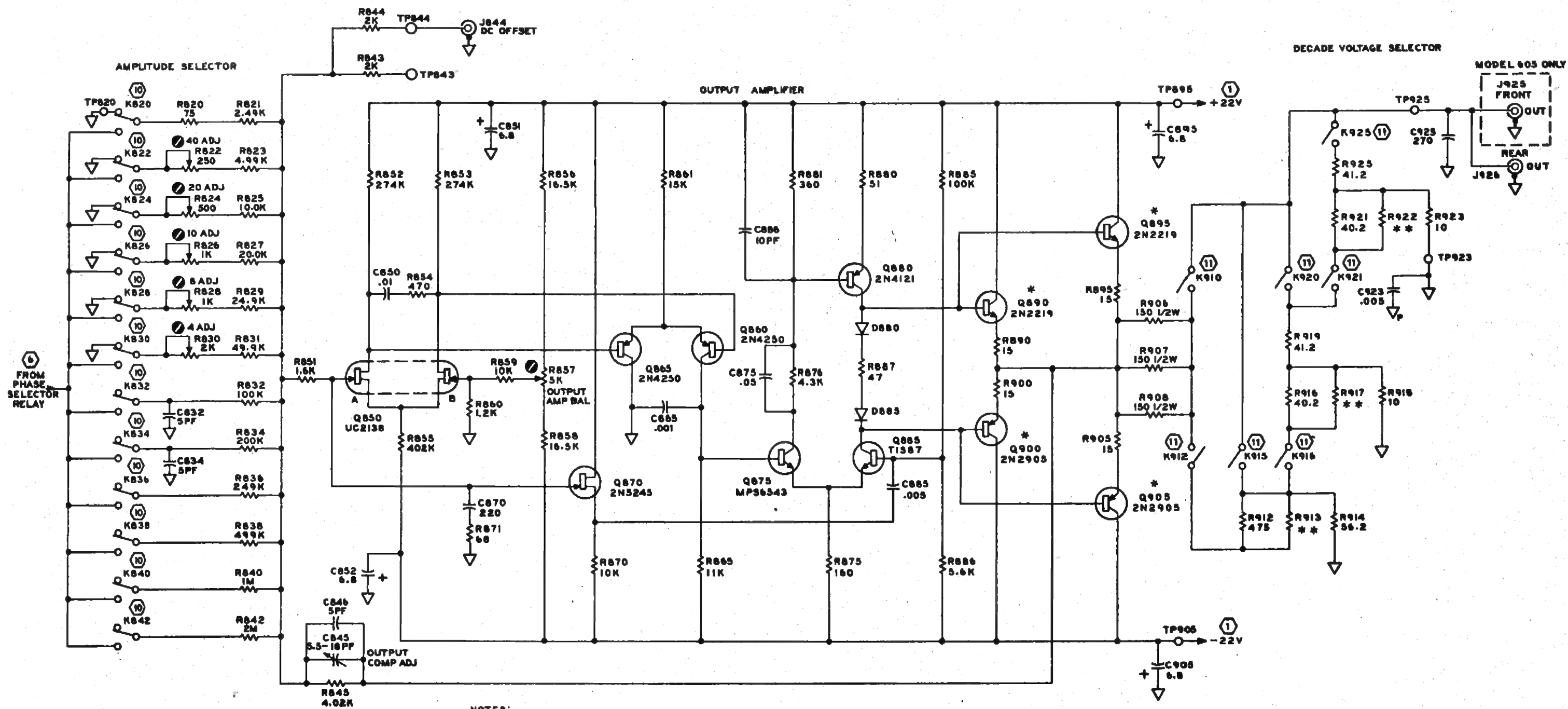
- NOTES:
 UNLESS OTHERWISE SPECIFIED
 1. ALL RESISTORS ARE IN OHMS
 2. ALL CAPACITORS ARE IN MICROFARADS
 3. ALL DIODES ARE IN914
 4. ALL IC'S ARE SN7400N
 5. ISOLATED PROGRAMMING COMMON
 6. J1300 PROGRAMMING INPUT CONNECTOR

FIGURE 8.2.7
 SCHEMATIC DIAGRAM MODEL 605-606
 FUNCTION CONTROL CIRCUITS
 10-18-71



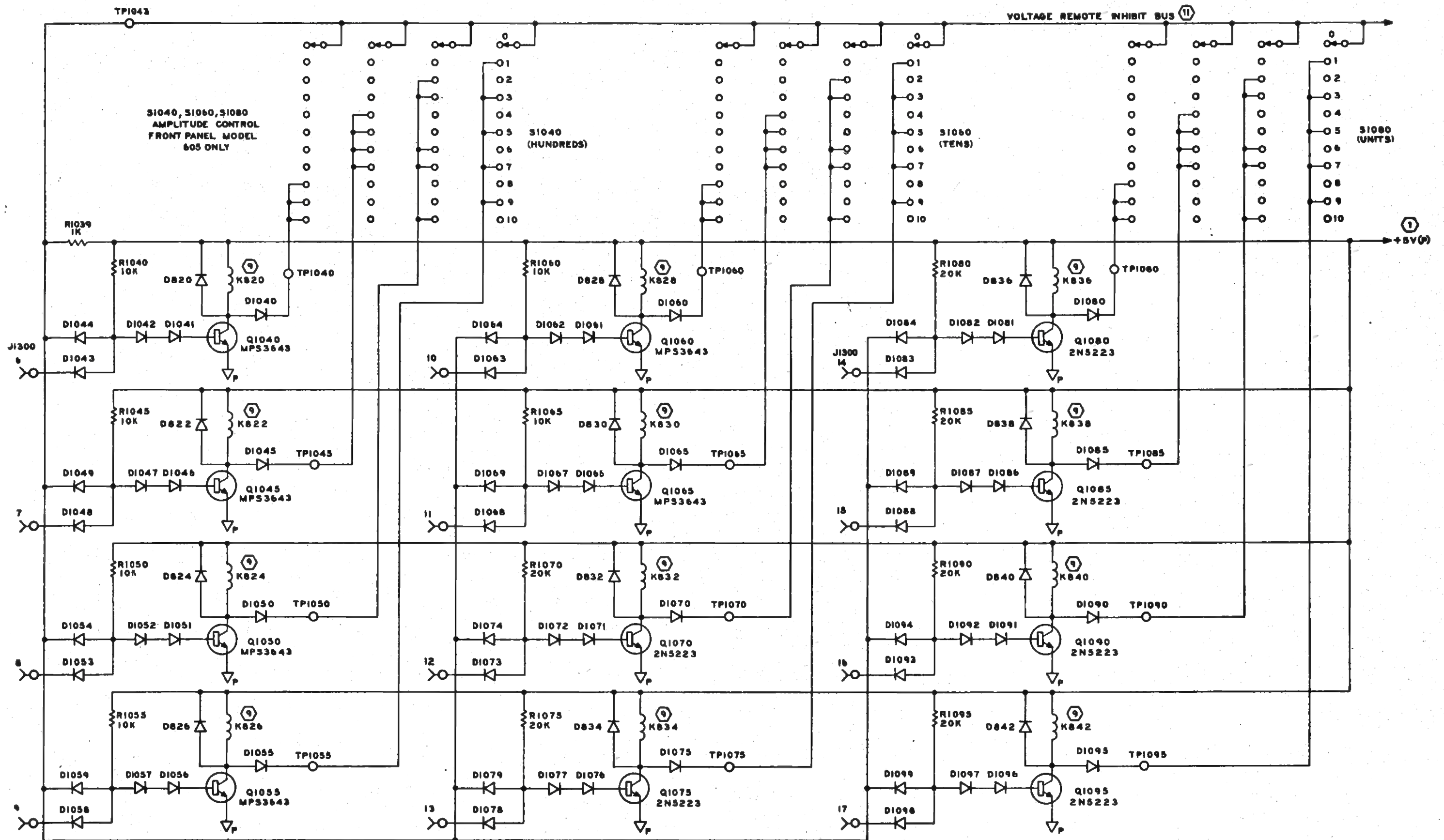
- NOTES:
 UNLESS OTHERWISE SPECIFIED
 1. ALL RESISTORS ARE IN OHMS
 2. ALL CAPACITORS ARE IN MICROFARADS
 3. ALL DIODES ARE IN914
 4. ALL IC'S ARE SN7400N
 5. ∇_P ISOLATED PROGRAMMING COMMON
 6. J1300 PROGRAMMING INPUT CONNECTOR

FIGURE B.2.B
 SCHEMATIC DIAGRAM MODEL 605-606
 FUNCTION & TRIGGER MODE INPUT CIRCUITS
 11-18-70 REV A



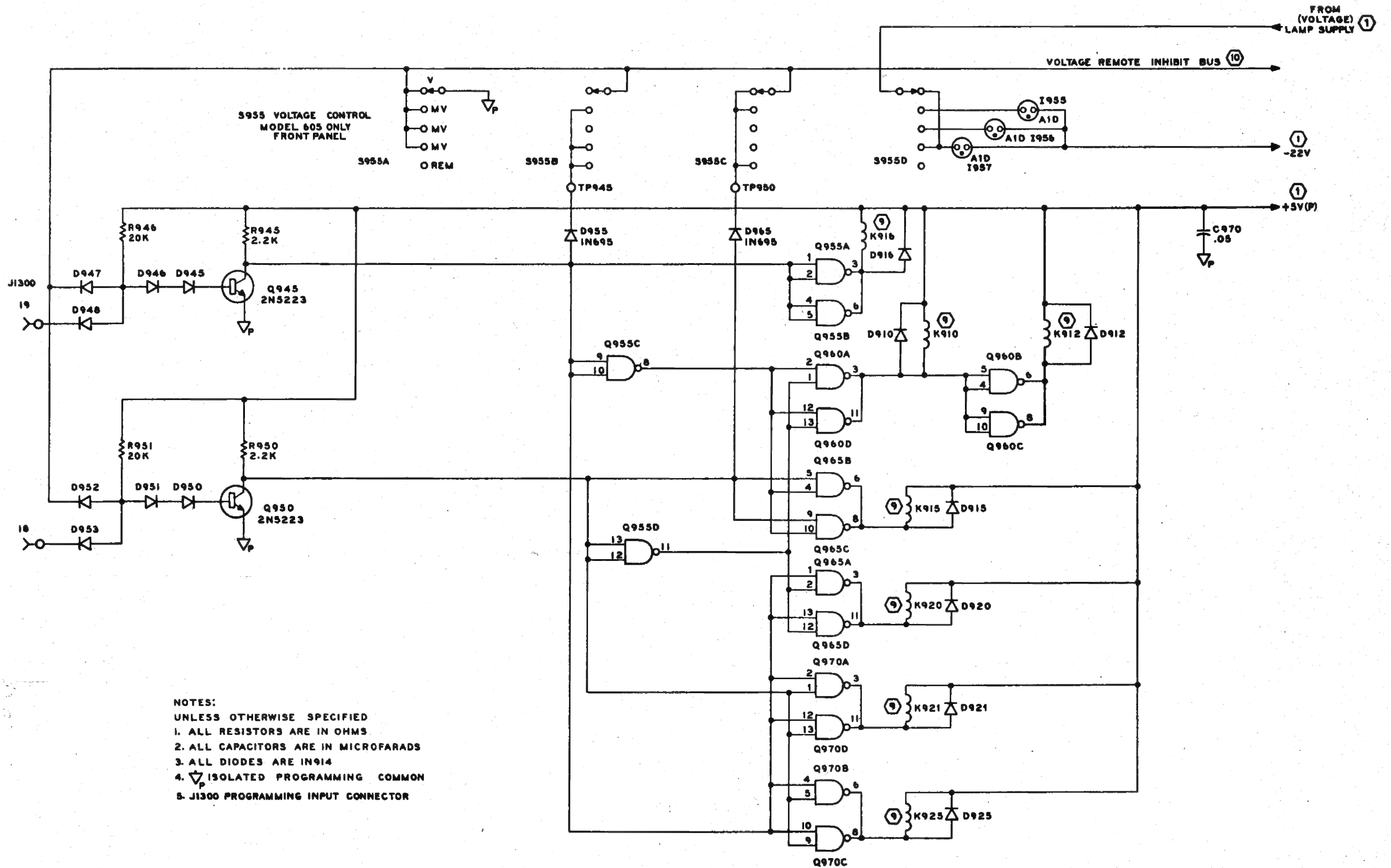
- NOTES:
 1. ALL RESISTORS ARE IN OHMS
 2. ALL CAPACITORS ARE IN μ F
 3. ALL DIODES ARE IN914
 4. ∇ CIRCUIT COMMON
 5. * HEAT SINK
 6. ** SELECTED AT FACTORY

FIGURE 8.2.9
 SCHEMATIC DIAGRAM MODEL 605-606
 OUTPUT AMPLIFIER CIRCUIT
 11-18-70 REV. (A)



- NOTES:
 UNLESS OTHERWISE SPECIFIED
 1. ALL RESISTORS ARE IN OHMS
 2. ALL CAPACITORS ARE IN MICROFARADS
 3. ALL DIODES ARE IN914
 4. ∇ ISOLATED PROGRAMMING COMMON
 5. J1300 PROGRAMMING INPUT CONNECTOR

FIGURE 8.2.10
 SCHEMATIC DIAGRAM MODEL 605-606
 OUTPUT VOLTAGE CONTROL
 10-16-71



NOTES:
 UNLESS OTHERWISE SPECIFIED
 1. ALL RESISTORS ARE IN OHMS
 2. ALL CAPACITORS ARE IN MICROFARADS
 3. ALL DIODES ARE IN914
 4. ∇_P ISOLATED PROGRAMMING COMMON
 5. J1300 PROGRAMMING INPUT CONNECTOR

FIGURE 8.2.11
 SCHEMATIC DIAGRAM MODEL 605-606
 DECADE VOLTAGE CONTROL
 11-18-70